EK-DR11W-UG-001

DR11-W Direct Memory Interface Module

User's Guide

digital

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User's Guide

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CHAPTER 1
INTRODUCTION

1.1 GENERAL

The DR11-W DMA Interface Module M8716 User's Guide provides the following information:

- General Introduction
- Programming Details (Software Interface)
- Description of I/O Signals
- Theory of Operation
- Interface Considerations
- Installation Procedures
- Interprocessor Lines (Link Mode Operation)
- Corrective-Maintenance Diagnostics Listing

1.2 SUPPORTING DOCUMENTATION

Two support documents are available for use with this User's Guide:

1. Field Maintenance Print Set (MP00693)
2. *PDP-11 Bus Handbook* (EB17525-20/79-07-14-55)

1.3 FUNCTIONAL DESCRIPTION

The DR11-W is a general-purpose, UNIBUS, direct memory access (DMA) device whose principal performance characteristics are listed in Table 1-1. The DR11-W (Figures 1-1 and 1-2):

1. Provides the means to connect a user device to the UNIBUS of a PDP-11 or VAX computer in either single- or multiple-DR11-W system configurations.

2. Provides the means to link a PDP-11 or VAX system with other PDP-11 or VAX systems.

3. Can be connected to a DRV11-B to provide a UNIBUS to Q-Bus system link.

An unlimited number of DR11-Ws can be used in a system if the addresses and vector selected for each device do not conflict with the addresses and vectors of other devices.

The DR11-W is designed for installation in a single hex small peripheral controller (SPC) slot of a system backplane located within the same enclosure, and is connected to the user device, a DRV11-B, or another DR11-W by not more than 50 feet of cable.

In response to software commands, the DR11-W is capable of crossing 32K boundaries to transfer a maximum block of 64K 16-bit words. Table 1-2 gives nominal transfer rates for typical processor configurations (Figure 1-3.)

Table 1-1 DR11-W Performance Specifications

Item	Description
Data Transfer:	
Format	16-bit word (parallel transfer)
Modes	Programmed data DMA block (1 cycle, 2 cycles or N cycles per bus grant)
Types	DATI (Read word) DATIP (Read word with Write to same address to follow) DATO (Write word) DATOB (Write byte)
Addressing capacity	128K words
Maximum block size	64K words (can cross 32K UNIBUS boundaries)
Transfer rate	See Table 1-2
User Burst Data Late Timeout	Adjustable from 4 to 40 μsec to accommodate input data rate (10 to 15 usec is a nominal setting)
Bus Timeout	18 μsec, nominal
Bus Interrupt Priority	Plug selectable for BR4 to BR7 (BR5 is supplied with DR11-W)
Switchpacks:	
Operational Mode Selection Bus Address Vector Address	Switchpack E105 – 5 switches Switchpack E120 – 10 switches Switchpack E15 – 8 switches
I/O Signal Lines:	
To User Device From User Device	25 28
Cables:	
DR11-W/User Device Interconnect	2 BC06R-XX 40-conductor, 120-ohm, 1524 cm (50 ft), max.
Maintenance Wraparound	1 BC05L-1C 40-conductor, 120-ohm 38 cm (15 in.)
Temperature:	
Ambient Operating Storage	5 to 50°C (41 to 122°F) −40 to 66°C (−40 to 151°F)
Humidity	10 to 90% noncondensing with max. wet bulb 32°C (90°F) and minimum dew point 2°C (36°F)
DC Power	+5 Vdc @ 3.7 A, nominal

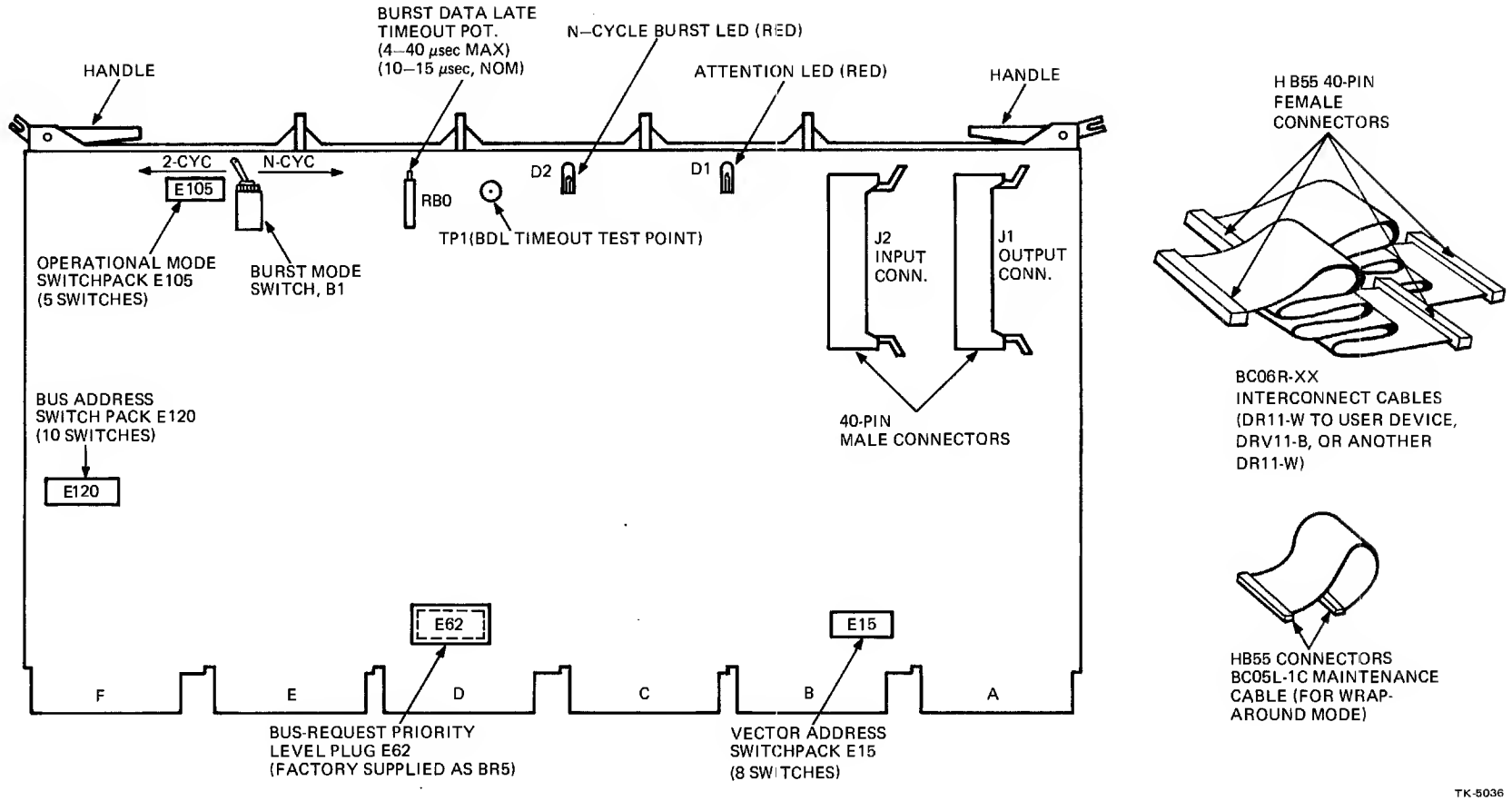


Figure 1-1 DR11-W DMA Module M8716

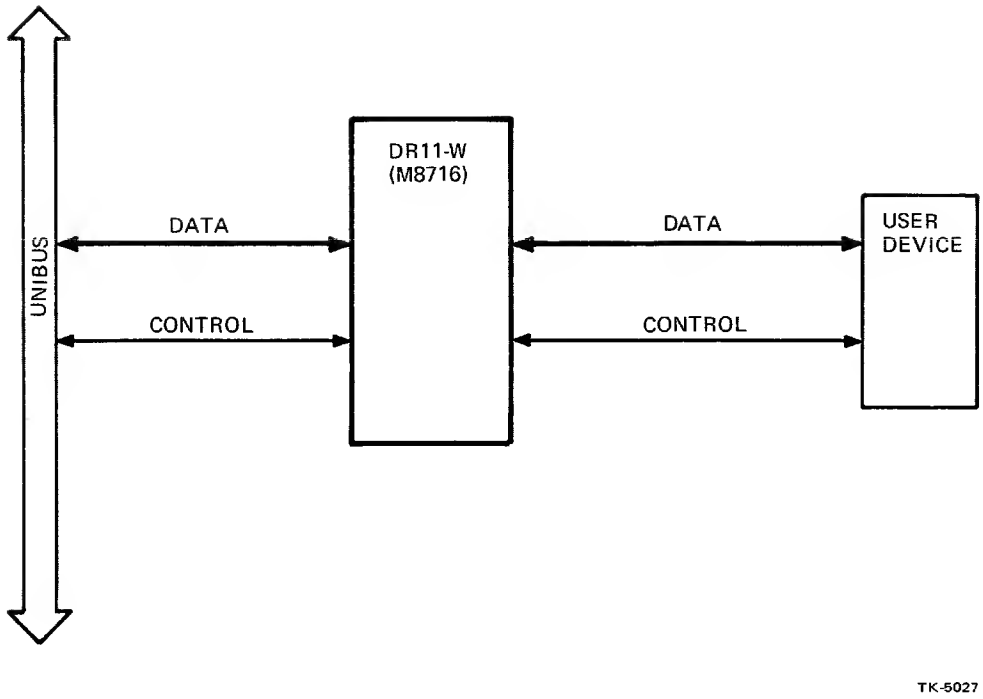


Figure 1-2 Simplified Block Diagram of DR11-W Used as Interface for UNIBUS and User Device

Table 1-2 Nominal Transfer Rates for Typical Processor Configurations

	DR11-W UNIBUS	DR11-W UBA	DRV11-B LSI Bus
DR11-W UNIBUS	500K wps	300K wps	250K wps
DR11-W UBA	300K wps	400K wps	250K wps
DRV11-B LSI BUS	250K wps	250K wps	Not applicable

Figure 1-2 is a simplified block diagram showing the DR11-W used in a configuration with a UNIBUS and a user device. Figure 1-3 summarizes the DR11-W's use in more complex arrangements that enable use of a VAX or PDP-11 with another VAX or PDP-11. Figure 1-4 is a simplified functional block diagram for these applications of the DR11-W.

The DR11-W can be operated in either a programmed I/O or DMA mode. In programmed I/O, data is moved to or from the user device under CPU program control. When operated in DMA mode, the DR11-W becomes bus master via an NPR request and operates directly on the memory to satisfy requests originated at the user device.

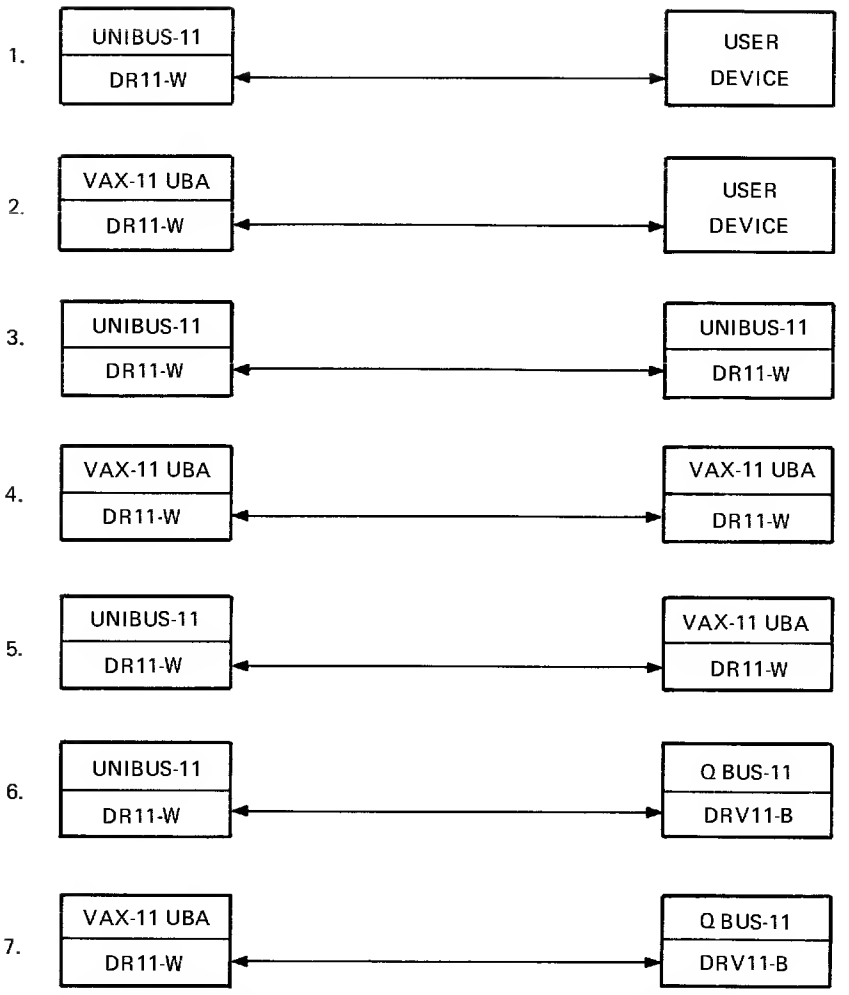


Figure 1-3 Interface Configurations

A normal DMA operation transfers one word per UNIBUS arbitration. However, DMA operation can be extended to include transfers in either standard or nonstandard burst modes. In the standard burst mode, two words are transferred at the completion of each UNIBUS arbitration in which the DR11-W is granted the bus. In nonstandard burst mode operation, an unlimited number of words can be transferred after receipt of each bus grant.

The DR11-W detects memory parity errors during DATI (read word) and DATIP (read word with intent to write same address) DMA transfers only. Error detection generates an interrupt at the end of the current cycle and terminates the DMA operation. The error is cleared at the start of the next DMA transfer.

For burst mode operation, optimization of DMA latency for each application is individually effected using a screwdriver-adjusted potentiometer on the M8716 board.

DR11-W interruption of the CPU at any one of four priority levels (BR4 – BR7) is possible. A BR plug (normally supplied as BR5 for the DR11-W) provides this interrupt capability.

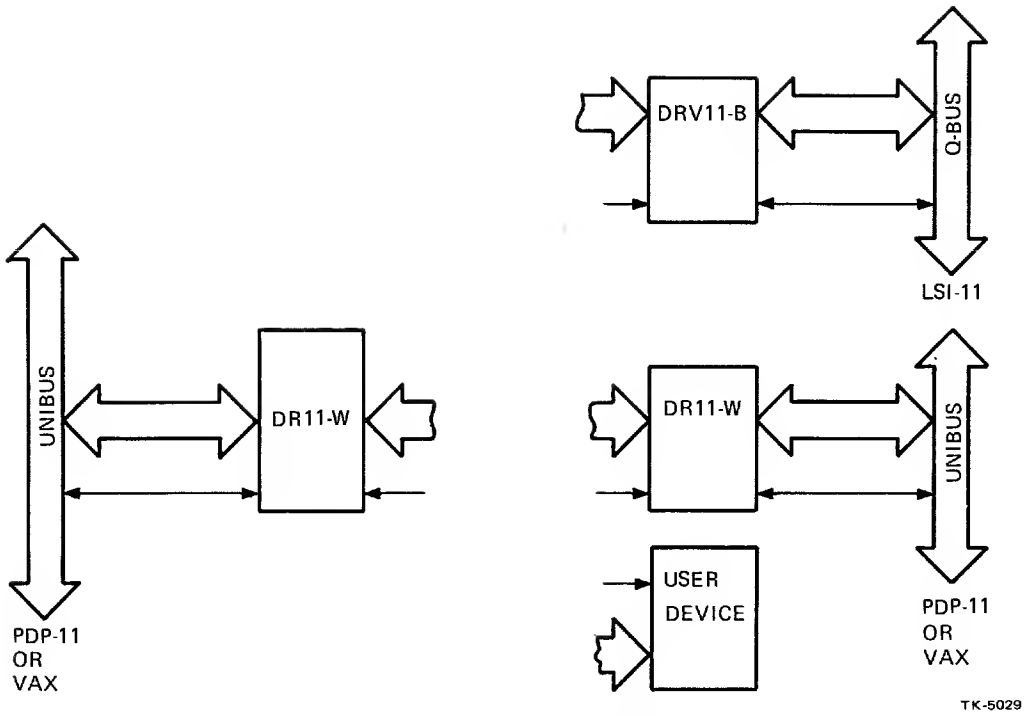


Figure 1-4 Simplified Block Diagram for DR11-W Used in Typical Configurations

1.4 MAINTENANCE MODES

The DR11-W can be tested in either of two maintenance modes:

1. Logic wraparound
2. Cable wraparound

In logic wraparound testing, UNIBUS data applied to the module is gated back to the UNIBUS for comparison checking. In this mode, all DR11-W components, except the I/O connectors and transceivers, are checked for satisfactory operation.

NOTE

Since random external patterns are generated during this operation, the user device may need to be isolated from the DR11-W until testing is completed.

In cable wraparound testing, a BCO5L test cable (see Paragraph 1.6) is installed between the J2 input connector and the J1 output connector, so that data is looped back to the module. This provision checks the I/O connectors and transceivers of the DR11-W.

1.5 COMPATIBILITY OF DR11-B AND DR11-W

The DR11-W has two modes of operation: DR11-B mode and DR11-W mode. Both modes are set by DIP switch 5 (E105 in Figure 1-1). In its DR11-B mode, the DR11-W is both functionally and software compatible with the DR11-B; refer to Appendix C for minor differences between the two interfaee modules.

The DR11-W mode provides additional error-condition monitoring and enables the interprocessor link capability. Programming the device in DR11-W mode is only slightly different from its programming in the DR11-B mode.

For PDP-11, the DR11-W is supported in both modes by diagnostics for the User-Device and interprocessor-link applications. Like the DR11-B, there is no operating system support for the DR11-W.

For VAX, the DR11-W is supported (in DR11-W mode only) by diagnostics and the VAX/VMS operating system.

1.6 PHYSICAL DESCRIPTION

Figure 1-1 shows the relative location of the DR11-W components whose adjustment or indicator status is significant to the user during operational setup and troubleshooting. The DR11-W is configured as a standard hex-height, multilayer, high-density module carrying the designation M8716.

The DR11-W connects to the user device via two BC06R-XX cables. Each end of each cable is terminated by a 40-pin connector; cable impedance is 120 ohms. The BC06R-XX cable is 1524 cm (50 ft) long, the maximum recommended length for this application.

NOTE

Approved interface cables other than DEC standard BC06R-XX (bare cable DIGITAL P/N 17-00034-00) are Tensolite (P/N) 81-25-00-4000) or an equivalent cable from Spectrastrip, 3m, or Brand Rex.

The DR11-W components whose settings or status indications are of interest to the user during installation, operation, and troubleshooting are (Figure 1-1):

1. Three dual in-line switchpacks:

   E15 - vector address (eight switches, but switch 1 not used)
   E105 - operational mode (five switches)
   E120 - bus address (ten switches)

2. Burst mode toggle switch B1 (2 Cycle/N cycle)

3. N-cycle burst LED (Red)

4. ATTENTION LED (Red)

5. E62 priority jumper (normally supplied for BR5 priority)

6. Burst data late timeout potentiometer

7. Burst data late calibration test point (TP1)

8. Six programmable registers:

Address	
7XXXX0	word count register (WCR)
7XXXX2	bus address register (BAR)
7XXXX4	control and status register (CSR)
7XXXX4	error and information register (EIR) (DR11-W mode only)
7XXXX6	input data register (IDR)
7XXXX6	output data register (ODR)

The names of the vector address switchpack (E15), and the bus address switchpack (E120), denote their functions. The operational mode switchpack (E105) permits user selection of BUSY, CYCLE INHIBIT, READY, and DR11-B/DR11-W mode.

The burst mode toggle switch is set for standard (2-cycle) or nonstandard (N-cycle) mode, as desired. The switch position for each mode is indicated by lettering on the component side of the board adjacent to the switch.

The N-cycle burst LED illuminates whenever the burst mode switch is set to the N-cycle position and an NPR transfer is in progress.

The ATTENTION LED illuminates whenever a user device generates an attention signal, or the DR11-W input cable is disconnected from the DR11-W or the user device.

The burst data late timeout potentiometer is adjustable over the range of 4 to 40 μsec.

NOTE
For the VAX operating system to handle UBA zero-vector interrupts, timeout should not exceed 20 μsec.

Priority plug E62 enables selection of priority level BR4, 5, 6 or 7. BR5 is the standard plug supplied with the DR11-W module.

CHAPTER 2
SOFTWARE INTERFACE

2.1 GENERAL

The DR11-W uses six programmable registers (see Paragraph 1.5 for their respective addresses). The IDR and ODR, being at the same physical address, are grouped under a single main heading below. For the same reason, the CSR and EIR are grouped under a common main heading. The WCR and BAR, at different addresses, are discussed under separate main headings.

2.2 WORD COUNT REGISTER (WCR)

The WCR is the first register on the DR11-W. If the DR11-W is addressed at 772410, the WCR address is also 772410. The WCR can be read or written by the CPU, and is cleared during initialization.

Prior to a data transfer, the WCR is loaded with the two's complement of the total number of words to be transferred. During subsequent transfers, the WCR is incremented by one for each word transferred. Upon transfer of the last word, the WCR overflows and causes the READY flip-flop in the DR11-W control logic to set, an action that tells the user that his transfer is complete. If DR11-W interrupts are enabled, an interrupt occurs at this time.

2.3 BUS ADDRESS REGISTER (BAR)

The BAR, like the WCR, is word-addressable only. Continuing our example of the addressing hierarchy (see Paragraph 2.2), if the DR11-W is addressed at 772410, the address of the BAR will be 772412. The BAR can be read or written by the CPU, and is cleared during initialization. This register supplies 15 of the 18 bits used as the UNIBUS address during NPR transfers by the DR11-W. The full 18-bit address, BA(17:00), is derived as follows:

1. Bits BA(17:16) are provided by CSR bits 5 (XBA17) and 4 (XBA16), respectively.
2. Bits BA(15:01) are provided by BAR bits (15:01), respectively.
3. BA(00) is generated by the User Device as A00.

In link operation, the READY output of each DR11-W is coupled to the A00 input of the other DR11-W. To prevent operation at an odd address, switch 4 of the operational mode switchpack E105 is set to ON, thereby grounding the A00 input.

The BAR is normally incremented by two after an NPR data transfer, so that succeeding transfers are made to consecutive words; i.e., the bus address is advanced by two byte-address increments after each transfer. A user device can also select byte transfers by sending the following control signals to the DR11-W: A00 H, C0 CNTL H, and BA INC ENB H.

When the BAR overflows to all 0's, extended bus address bits XBA17 and XBA16 are incremented. This provision enables transfers across 32K word boundaries.

2.4 INPUT DATA REGISTER/OUTPUT DATA REGISTER (IDR/ODR)

The input and output data registers share the same address. Continuing our example (in Paragraphs 2.2 and 2.3), if the DR11-W is addressed at 772410, the address of the IDR/ODR is 772416. Writing to this address loads the ODR; reading from this address gives the contents of the IDR. This register is cleared during initialization.

2.4.1 Input Data Register (IDR)

During writes to the memory, the IDR buffers data received from the user device. In the programmed I/O mode, the program can obtain this data by reading the IDR. The IDR is read to the bus as DI(15:00).

Upon completion of a data transfer, the CPU can examine the last word transferred by reading the IDR. This can only be done by writing a 1 to bit 15 of the CSR register to set the EIR ENB flip-flop in the control logic. If the IDR is read with EIR ENB cleared, new data will be sampled from the user device and clocked into the IDR. The CPU then reads this new data. Note that EIR functionality is available in the DR11-W mode only (it is inhibited in DR11-B mode to effect compatibility).

During operation in the maintenance-logic wraparound mode, the contents of the ODR are clocked into the IDR at the end of the DATI cycle. This data is therefore available for the subsequent DATO cycle.

2.4.2 Output Data Register (ODR)

The ODR can be written to, but not read. When the CPU writes to the IDR/ODR address, the ODR is loaded. This register is also loaded during NPR transfers whenever the DR11-W reads from memory. The ODR contents are read to a user device as DO(15:00) H. The ODR is cleared during initialization.

2.5 CONTROL AND STATUS REGISTER/ERROR AND INFORMATION REGISTER (CSR/EIR)

The CSR and EIR share the same address. Continuing our example (Paragraphs 2.2, 2.3 and 2.4), if the DR11-W is addressed at 772410, the CSR/EIR address is 772414. Writing to this address always writes to the CSR; the EIR is a read-only register. Reading from this address accesses the content of either the CSR or EIR, as described below. Note again that the EIR is enabled in DR11-W mode only.

In writing to bit 15, the following rules apply:

1. Writing a 0 results in:

    a. The CSR bits are read
    b. Bit 0 from this address always reads 0

2. Writing a 1 results in:

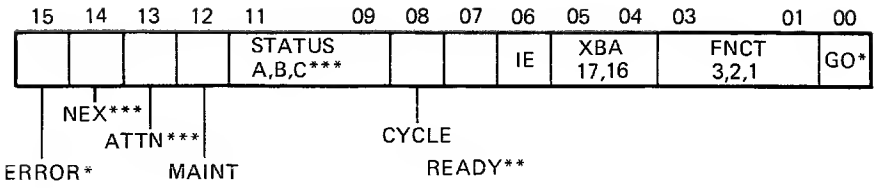
    a. The EIR bits are read
    b. Bit 0 always reads as a 1.

2.5.1 Control and Status Register (CSR)

Figure 2-1 shows the bit configuration of the CSR; the name and function of each bit is given in Table 2-1.

2.5.2 Error and Information Register (EIR)

Figure 2-2 shows the bit configuration of the EIR; the name and function of each bit is given in Table 2-2.



NOTES:

1. BITS WITH NO ASTERISK ARE READ/WRITE
2. BITS WITH A SINGLE ASTERISK CAN BE WRITTEN AS "1" BUT ARE ALWAYS READ AS ZERO ("0")
3. BITS WITH A DOUBLE ASTERISK ARE READ ONLY
4. BITS WITH A TRIPLE ASTERISK ARE READ/CLEAR.

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Figure 2-1 Control and Status Register (CSR)

Table 2-1 CSR Register: Bit Functions

Bit	Name	Function
00	GO	This bit is written under program control and is always read to the bus as zero. Setting this bit causes the DR11-W to begin its transfer.
(3:1)	FNCT 3 FNCT 2 FNCT 1	These function bits are user-defined, and specify the operation the user intends to perform. They are read/write, and cleared during initialization.
(5:4)	XBA17 XBA16	These bits generate extended BUS A(17:16) for NPR transfers, and are incremented when the bus address register overflows. They are read/write, and cleared during initialization.
6	IE	The interrupt enable (IE) bit, when set, allows an interrupt to occur if: • A GO pulse is generated after an error has been detected. • The word count register overflows at the end of a transfer. • An error condition signal is detected (i.e, ERROR, NEX, ATTN, ACLO, MULTICY RQ, or PAR ERROR) during an NPR transfer. • A user device error signal (ATTN) is sent to the DR11-W. IE is a read/write bit and is cleared during initialization.
7	READY	READY is a read/write bit. When set, it indicates that the DR11-W has completed the previous operation and is ready to accept a new command. The ERROR bit must be checked to determine whether or not the transfer was successful. Any error condition must be cleared before a new command can be executed. READY is cleared by setting GO or by initialization.

Table 2-1 CSR Register: Bit Functions (Cont)

Bit	Name	Function
8	CYCLE	The CYCLE bit can be set under program control to initiate one NPR operation upon setting the GO bit. CYCLE is a read/write bit that is cleared during initialization, and at the start of a bus cycle.
(11:9)	STATUS A STATUS B STATUS C	These user-defined bits indicate user device status, are stored by the DR11-W, and are read-only.
12	MAINT	MAINT allows diagnostic testing of the DR11-W in the logic wraparound mode. When the MAINT, CYCLE, and GO bits are set, the DR11-W starts data transfers that continue until the word count register overflows. During maintenance-mode testing, the DR11-W does alternating DATI/DATO transfers at consecutive locations; i.e., a DATI from location X is followed in sequence by a DATO to location X+2, a DATI from location X+4, etc.. During a DATI cycle, the ODR is loaded by bus D(15:00). This data is transferred to the IDR at the end of the cycle, where it is available for the DATO to follow. The MAINT bit can also be used for software reset. When set, the maintenance mode is entered; when cleared, the DR11-W is initialized. The MAINT bit is read/write and is cleared by initialization.
13	ATTN	The user device controls the ATTN signal and, by its assertion, indicates the on-line presence of the device. When ATTN is set, an ERROR flag is generated in the DR11-W. If IE has been set, it causes an interrupt and, if a DMA transfer is in progress, the transfer is stopped at the completion of the current cycle. ATTN is a read/write bit that is cleared during initialization or at the start of the next DMA transfer. Thus, GO can be set while ATTN is set.
14	NEX	NEX (nonexistent memory) indicates that the DR11-W is attempting a transfer to or from a nonexistent bus address. NEX sets when the DR11-W asserts MSYN, but does not receive SSYN within 18 usec. NEX causes ERROR, terminates DMA operation, and if IE is set, causes an interrupt. NEX is a read/write bit that is cleared during initialization by writing a 0 to it, or by starting the next DMA transfer.
15	ERROR	ERROR is a read-only bit and is the inclusive-OR of ATTN, NEX, MULTICY RQ, ACLO, and PAR ERROR. When ERROR is asserted, it sets READY and prevents further DMA cycles. If IE is set, an interrupt occurs. The ERROR bit can only be cleared by removing the conditions that caused it to be set; i.e., ATTN, NEX, ACLO, MULTICY RQ. These bits are cleared at the start of the next DMA transfer. However, ATTN and NEX can also be cleared by writing a 0 to bits 13 and 14, respectively.

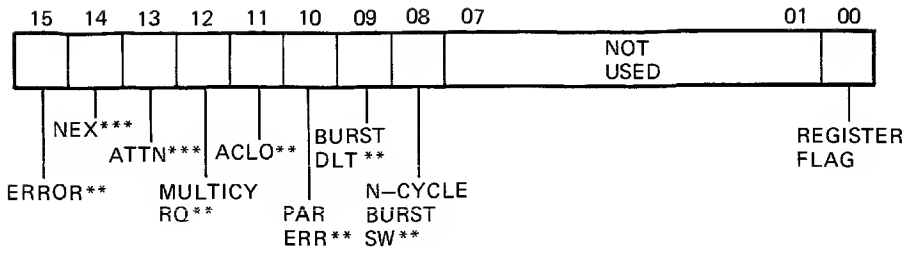

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Figure 2-2 Error and Information Register (EIR)

Table 2-2 EIR Register: Bit Functions

Bit	Name	Function
00	REGISTER FLAG	Bit 00 is a read-only bit. Reading a 1 in this bit confirms that the EIR, rather than the CSR, is being read.
(07:01)	Unassigned	Unassigned these bits are not used in the DR11-W. They read as 0 when the EIR is read.
08	N-CYCLE BURST	When set, bit 08 flags that the N-CYCLE/2-CYCLE burst mode switch is set in its N-CYCLE (nonstandard) position. When the DR11-W is configured to operate in burst mode, the N-CYCLE LED (see Figure 1-1) is lit whenever operation in burst mode is in progress.
09	BURST DLT	When bit 09 (burst data late) is set, it indicates that the user device has not supplied or removed data within the established time limit, and that the UNIBUS has been relinquished. The DR11-W is still ready to accept further cycle requests.
10	PAR ERR	Bit 10 (parity error) is set whenever the DR11-W detects a memory parity error during a memory read. Bit 10 clears at the start of the next DMA transfer.
11	ACLO	ACLO indicates that a powerfailure occurred during a DMA transfer. ACLO sets the error. It is cleared at the start of the next DMA transfer, or during initialization.
12	MULTICY RQ	Bit 12 (multicycle request) is caused by a user device that sends CYCLE RQ (A or B) to the DR11-W while the DR11-W is still processing a previous transfer. MULTICY RQ sets ERROR and is cleared at the start of the next DMA transfer.
15:13	ERROR, NEX, ATTN	Bits 15:13 are functionally the same as bits (15:13) of the CSR, but are displayed in the EIR for immediate access.

CHAPTER 3
I/O SIGNALS

Figure 3-1 shows the DR11-W I/O signal lines. Table 3-1 identifies and describes the functions of the 28 signals a user device sends to the DR11-W. Table 3-2 identifies and describes the functions of 25 signals a DR11-W sends to a user device.

NOTE
For the logic levels referenced in Tables 3-1 and 3-2, logical H is +3 V and logical L is 0.0 V (ground).

Figures 3-2 and 3-3 give the pin identifications for I/O output connector J1 and I/O input connector J2, respectively.

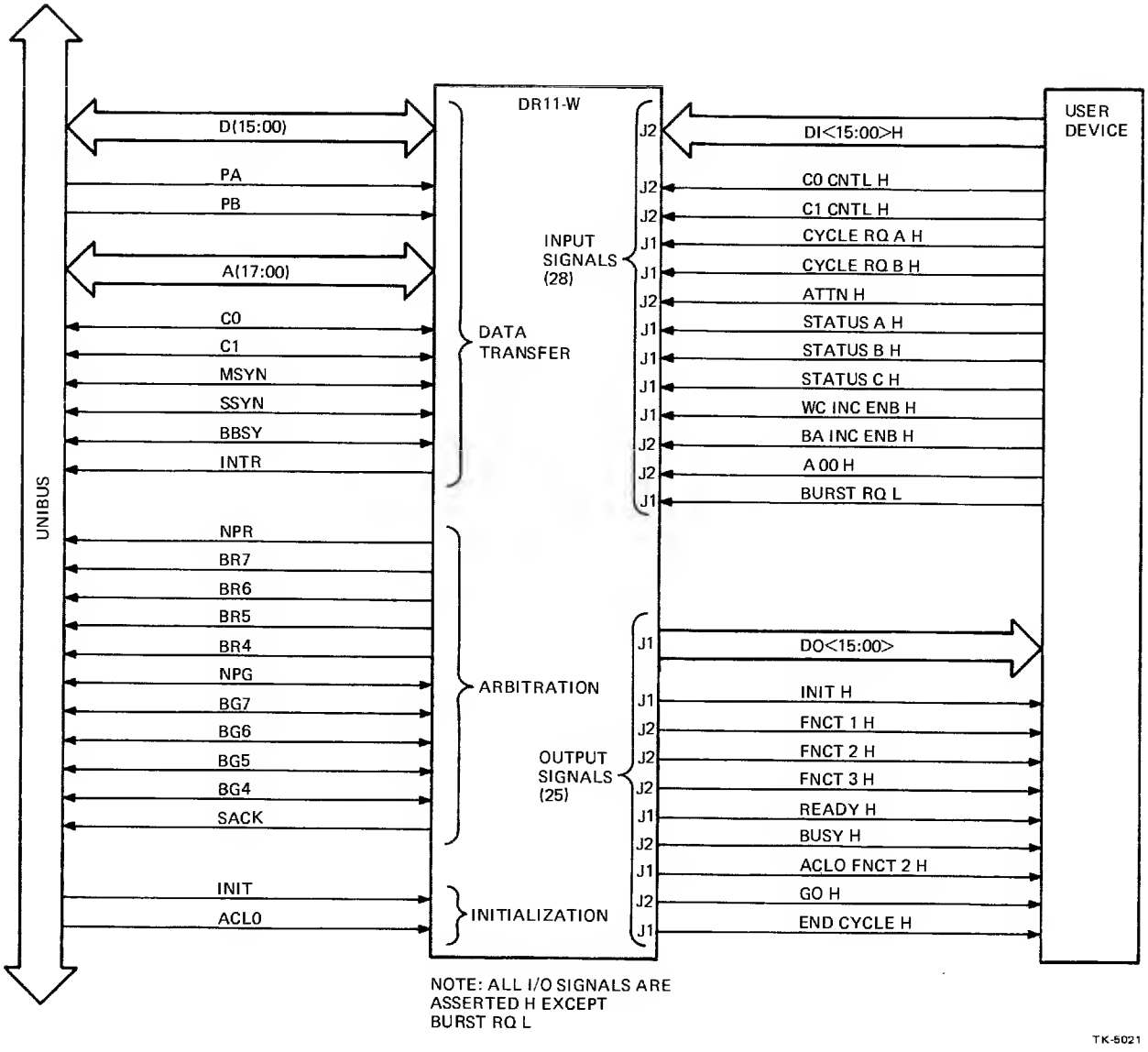

Figure 3-1 DR11-W I/O Lines

Table 3-1 Input Signals from User Device

Signal	Function
DI (15:00) H	User device data is transmitted to the DR11-W as DI(15:00). This data, buffered by the IDR in the DR11-W, may be read by the CPU or written to the memory in a DMA operation.
C0 CNTL H C1 CNTL H	User device encoding of these signals C1 determines which of the four possible types of bus cycle the DR11-W performs when it becomes bus master. These signals correspond logically to UNIBUS signals C0 and C1. The type of transfer is coded as follows: C0 CNTL H / C1 CNTL H / Cycle Performed 0 / 0 / DATI (Read word) 1 / 0 / DATIP (Read word with write to same address to follow) 0 / 1 / DATO (Write word) 1 / 1 / DATOB (Write byte)
CYCLE RQ A H CYCLE RQ B H	These signals (OR'ed together) are used independently to tell the DR11-W that the user device is requesting or presenting data.
ATTN H	ATTN (a user-defined signal) indicates that a user device error exists. When the current UNIBUS cycle is completed, ATTN causes ERROR to set, which in turn causes READY to set. ATTN can be read from the CSR as bit 13.
STATUS A H STATUS B H STATUS C H	These three signals indicate user device status; their application, however, is user-defined. They are read as part of the CSR.
WC INC ENB H	The word count increment enable signal allows the WCR to be incremented during each NPR transfer. If DATIP/DATOB cycles are performed, WC INC ENB should be negated for the duration of the DATIP cycles, or the even byte of the DATOB cycle, and every alternate cycle thereafter.
BA INC ENB H	The bus address increment enable signal causes the BAR to be incremented after each NPR transfer to conform with user requirements. Transfers may be made to the same location by holding this signal negated. If DATIP/DATOB cycles are performed, BA INC ENB must remain negated for the duration of the DATIP transfers or for the even bytes of the DATOB transfers.
A00 H	A00 specifies UNIBUS address bit <00> for NPR transfers. Thus, a user device can specify even or odd byte addresses. This signal must be negated for sequential word addressing.
BURST RQ L	If this signal is held asserted, the DR11-W operates in the NPR burst mode after it has become bus master.

Table 3-2 Output Signals to User Device

Signal	Function
DO (15:00) H	Data is transmitted from the DR11-W's output data register (ODR) as DO (15:00). When the DR11-W does a DATI, the ODR is loaded with data read from memory. This data is then sent to the user device.
INIT H	The initialization signal is sent by the DR11-W during power turn on/off, during the execution of a reset instruction, when the CPU is initialized from its front panel, or when the MAINT bit in the CSR is cleared.
FNCT 3 H FNCT 2 H FNCT 1 H	These signals from the DR11-W to the user device are based on CSR bits 3, and 1, respectively. They are user-defined, and specify a user device operation.
READY H	This signal corresponds to CSR bit 7 (READY).
BUSY H	BUSY H requires that switch 1 of operational mode switchpack E105 be set to ON, switch 2 set to OFF, and switch 3 set to OFF (see Table 6-4 and Figure 6-3). When BUSY H is at a logical 0 (L), it indicates to the user device that a DR11-W bus cycle has just been completed, and that the next user device request can be made. When BUSY is at a logical 1 (H), it indicates that a DR11-W bus cycle is in progress, and that no further requests can be made.
ACLO FNCT 2 H	This signal, generated by the DR11-W control logic, occurs only during a powerfail sequence, or when FNCT 2 is set. ACLO FNCT 2 indicates to the user device that a powerfail is about to occur. If a DMA transfer is in progress, an ERROR is generated. If an interrupt enable has been set, an interrupt will occur after the completion of the current cycle; any further DMA transfers are inhibited. If a DMA transfer is not in progress, ACLO FNCT 2 prevents any DMA transfers from being initiated.
GO H	GO is a 200 ns positive pulse that results from writing a 1 into the GO bit (bit 00) of the CSR. The GO pulse indicates that a new operation is to be performed.
END CYCLE H	END CYCLE is a 100 ns pulse that indicates the completion of a DR11-W UNIBUS cycle.

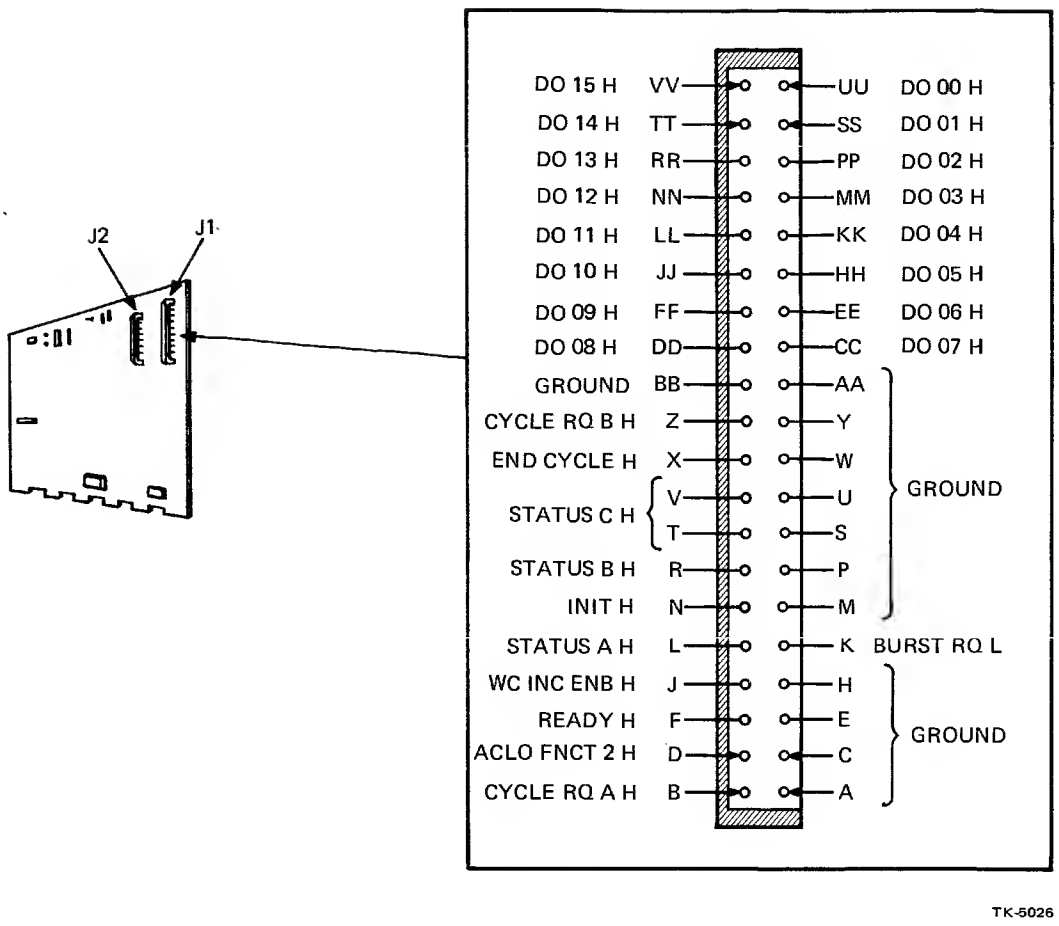

Figure 3-2 Output Connector J1: Signal Pin Assignments

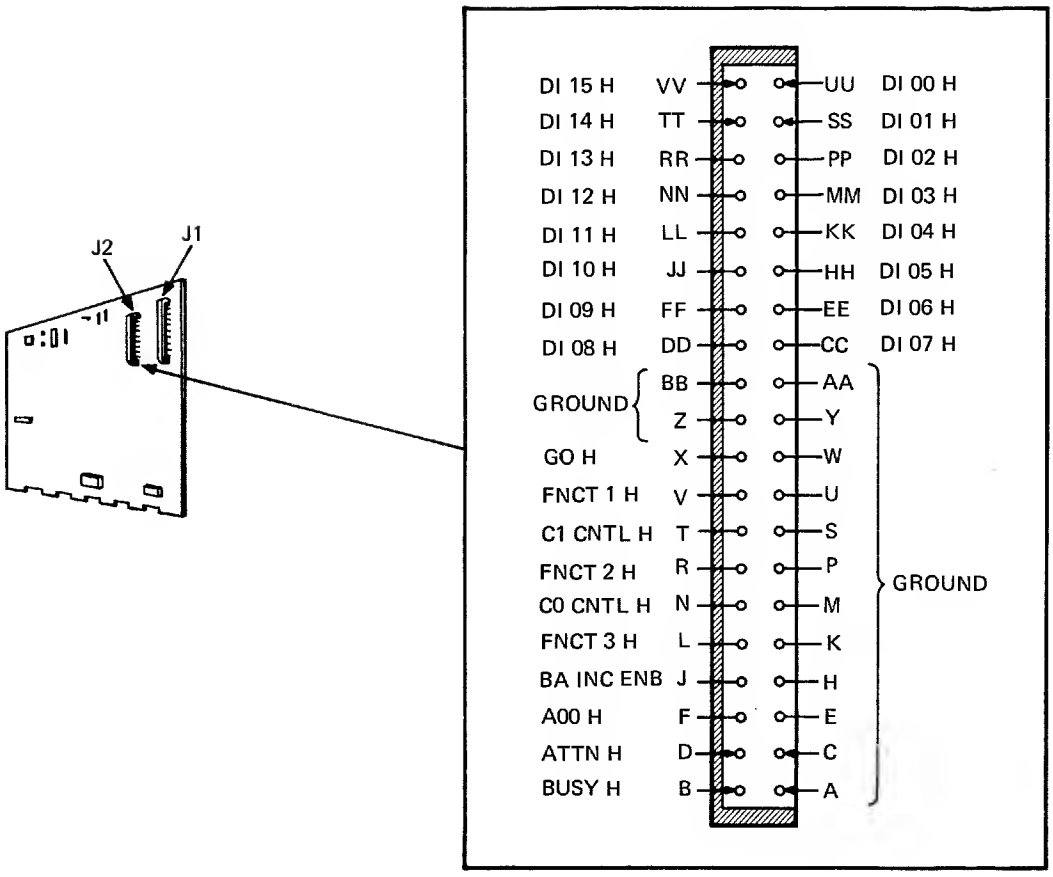

Figure 3-3 Input Connector J2: Signal Pin Assignments

CHAPTER 4
THEORY OF OPERATION

4.1 GENERAL

Figure 4-1 illustrates the DR11-W signal flow. As a general purpose DMA device, the DR11-W communicates directly with the memory by moving data between the UNIBUS (or UBA) and the user device. The DR11-W can also be used as an interprocessor link between two computer systems (see Figure 1-2 and Chapter 7, Interprocessor Links).

A user device receives UNIBUS data via the DR11-W output data register. DR11-W control signals are received from the UNIBUS via the DR11-W control logic. User device-generated data is routed through the I/O data multiplexer, input data register, and output multiplexer. This data is then applied to the UNIBUS via the bus drivers.

The control and status signals received by the DR11-W from the user device are applied to the I/O control multiplexer. Multiplexer outputs go to the input control register and the control logic.

The DR11-W has three operating modes:

1. Programmed data transfers, in which the CPU reads, or writes to, the DR11-W registers.

2. DR11-W interrupt of the CPU via a conventional bus request/bus grant sequence.

3. DMA data transfers to or from the memory with the DR11-W functioning as bus master after a nonprocessor request (NPR) and bus grant sequence.

4.2 PROGRAMMED DATA TRANSFERS

Programmed data transfers are basically program controlled. In this operating mode, the DR11-W functions as a slave to the CPU. The address of the DR11-W is defined by the settings of the bus address switchpack (E120) (Figure 4-2).

In the DR11-W address selection logic, REG SEL H is applied as an enabling input to a decoder that converts CPU coding of BA(02:01) H into one of four possible register select signals: LOAD BA L, LOAD WC L, SEL 4 L, or SEL 6 L. After the register is selected, CPU coding of BUS C0 L and C1 L determines whether a DATI/P or DATO/B transfer is to be performed. Only the CSR can be byte-written.

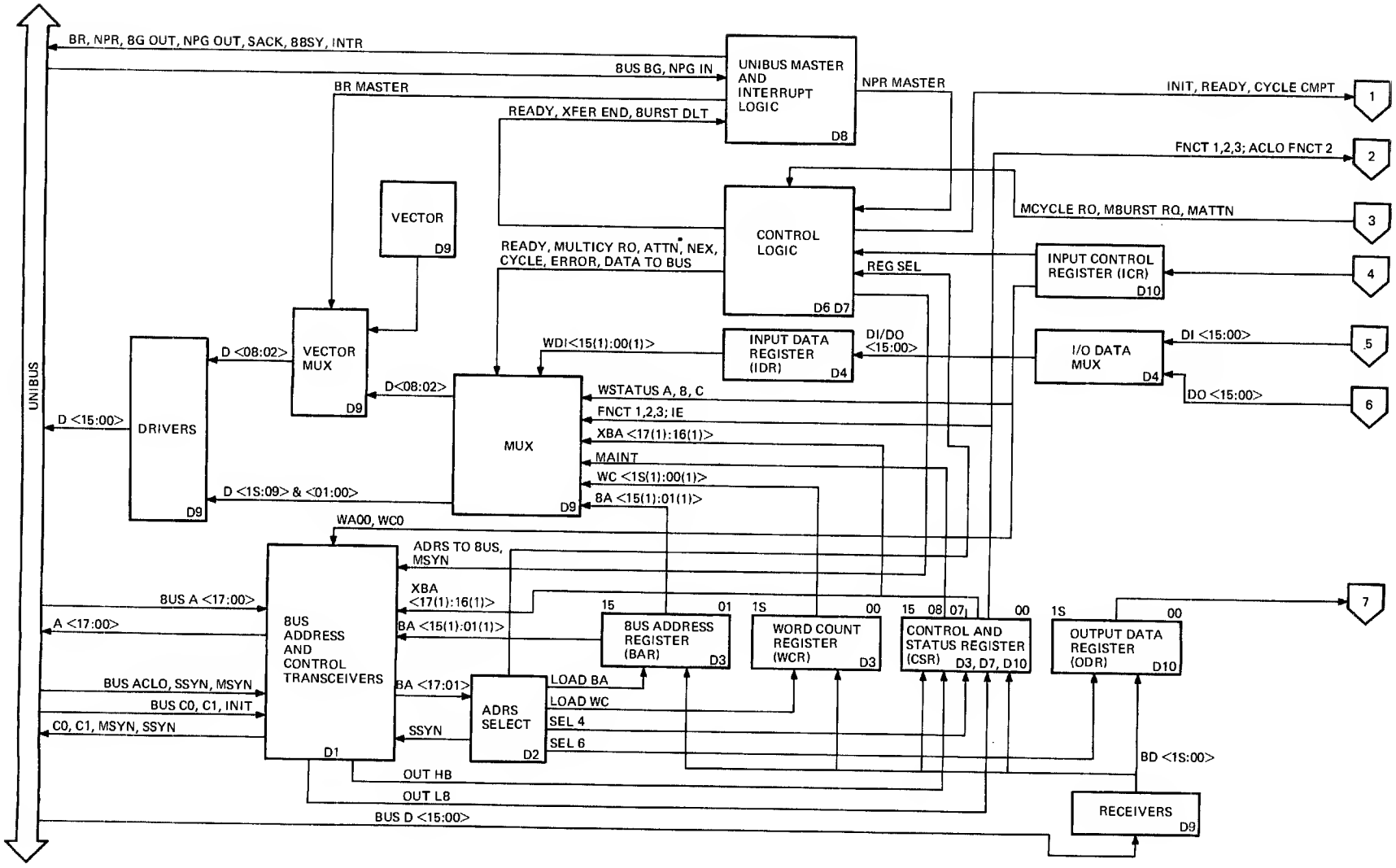

Figure 4-1 DR11-W Block Diagram (Sheet 1 of 2)

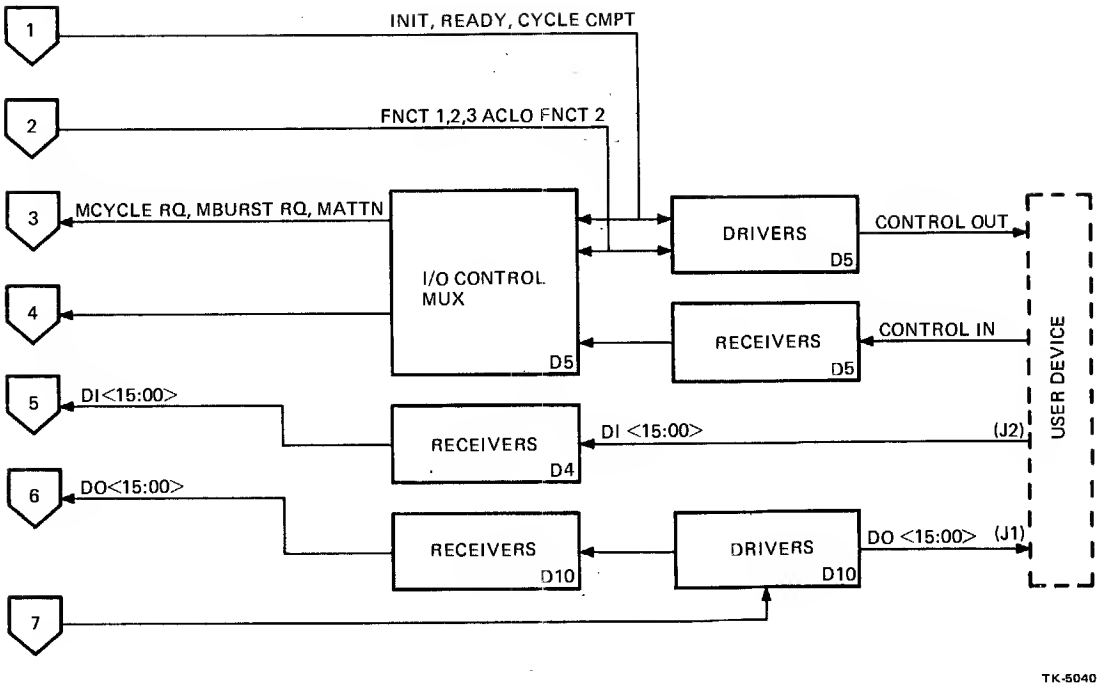

Figure 4-1 DR11-W Block Diagram (Sheet 2 of 2)

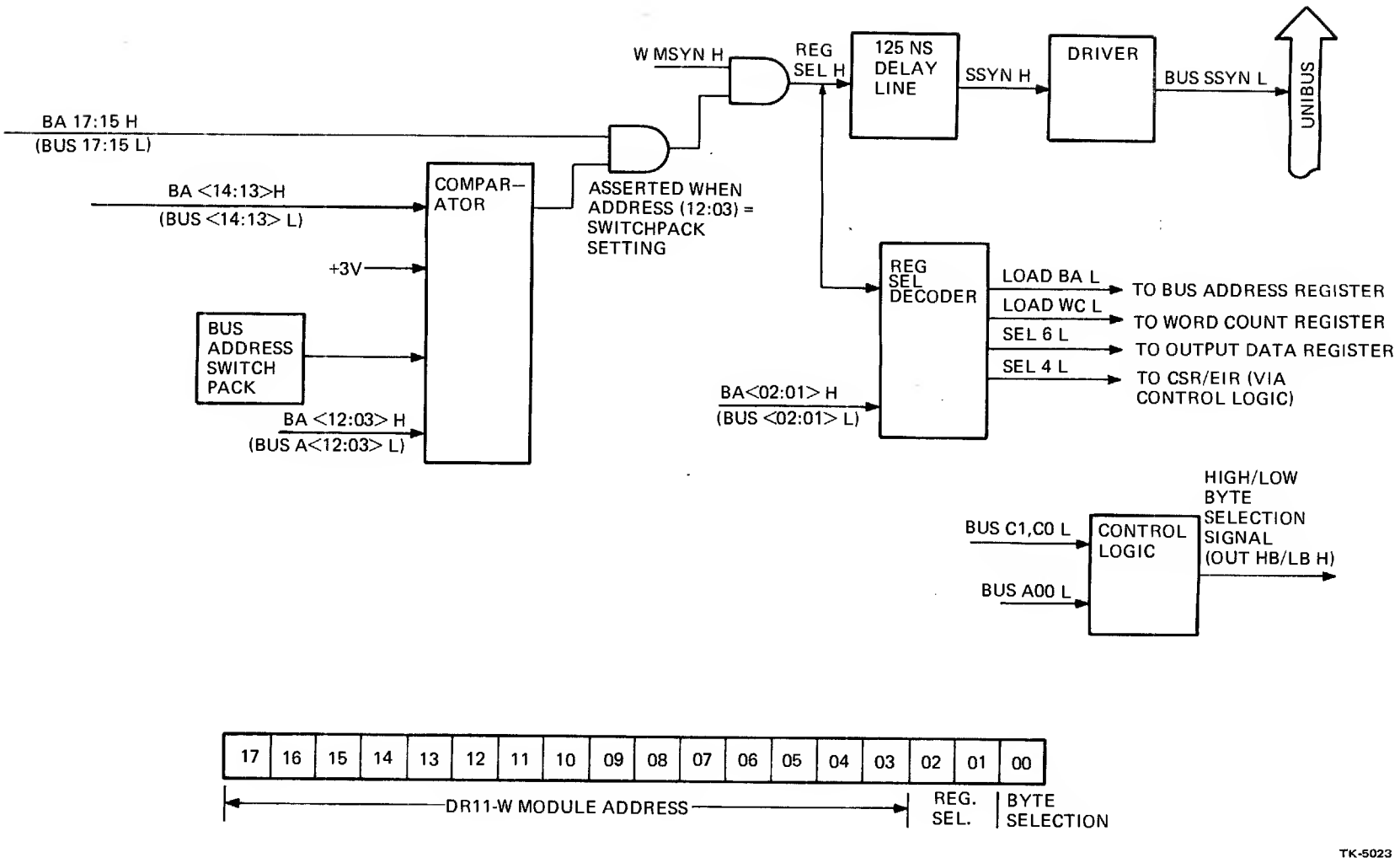

Figure 4-2 Address Decoding Logic

4.3 INTERRUPT OPERATION

Figure 4-3 shows the DR11-W interrupt logic; Figure 4-4 is the logic flow. The DR11-W interrupt level is user-selected by means of a priority-select plug. Four priority-select plugs are available (priority levels BR4, BR5, BR6 and BR7); BR5 is supplied with the DR11-W. The selected plug is inserted into socket E59 on the module. The following description of interrupt operation assumes that the plug (Part No. 54-8778) for priority level 5 (BR5) has been installed.

The outputs of the six flip-flops used for indicating errors (ACLO, PAR ERR, MULTICY RQ, ATTN, LINK ATTN, and NEX) are ORed together, then ANDed with the output of the interrupt enable (IE) flop to initiate an interrupt request. Note that, at the end of a transfer, the word count register (WCR) overflows and generates WCOF, which also causes an interrupt.

When an error is detected, the interrupt flip-flop causes an interrupt request to be generated. All DR11-W logic for processing interrupt requests is provided by a single DC013 chip. When the request is generated, the DC013 asserts BUS BR5 L via the priority interrupt plug. If the CPU is operating at priority level 4 or less, the signal BG5 H is asserted on completion of the current instruction. Then, if no higher-priority BR5 device is requesting service, the signal BUS GRANT propagates to the DR11-W. Upon receipt of BUS GRANT, the DR11-W asserts BUS SACK L to acknowledge its selection as the next bus master.

4.4 DMA OPERATION

The DR11-W becomes bus master (by generating an NPR) to effect the transfer of data between a user device and the UNIBUS. The user device controls the type of data transfer (DATI, DATIP, DATO or DATOB) by suitably coding control signals C0 and C1.

There are three DMA operating modes: block mode, 2-cycle (standard) burst mode, and N-cycle (non-standard) burst mode.

NOTE

N-cycle burst mode is not compatible with the VAX architecture, and therefore should not be used in any DR11-W/VAX configuration.

In block mode, the DR11-W must obtain, then release the bus for each word transferred; in burst mode, the DR11-W merely obtains bus master control, then holds it for a complete string of data transfers; i.e., for two cycles or an unlimited number of cycles (N cycles).

The block mode enables other devices on the bus to interleave their data transfers with those of the DR11-W. Transfers normally continue at a user-defined rate until the specified number of words has been transferred. (Timing diagrams reflecting the current revision status of the DR11-W are included in the DR11-W print set.)

During DMA transfers, the DR11-W control logic sends control signals (END CYCLE H, GO H, BUSY H, and READY H) to the user device via the lines leaving DR11-W output connector J1. The user device responds with data DI(15:00) H. This data reaches the DR11-W data multiplexer via the input control lines to connector J2 and the I/O receivers. The user device also generates several signals that are applied to the DR11-W I/O control multiplexer. These signals are:

- C0 CNTL H
- C1 CNTL H
- CYCLE RQ A (or B)
- WC INC ENB H
- BA INC ENB H, and
- BURST RQ L.

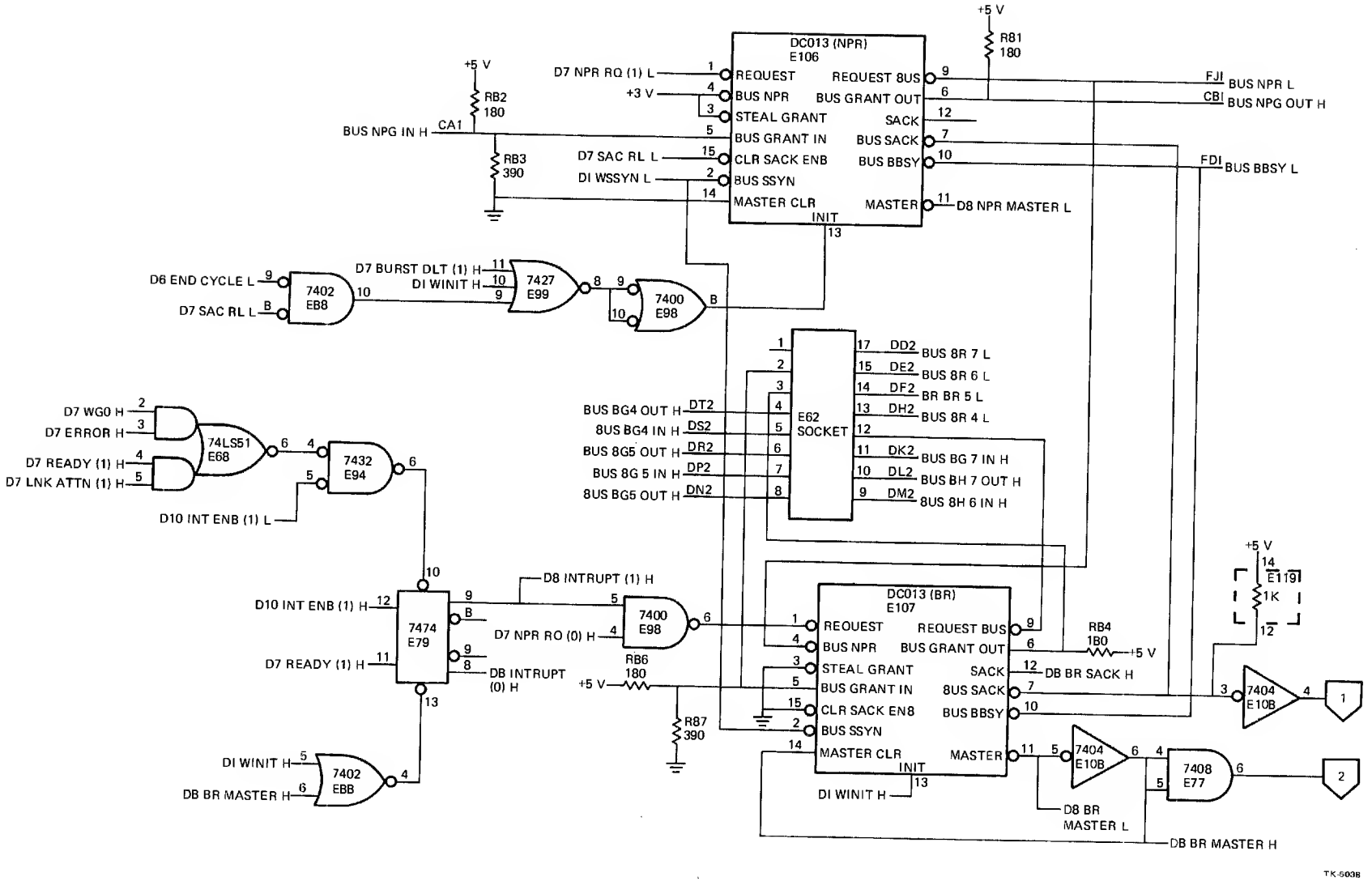

Figure 4-3 Interrupt Logic (Sheet 1 of 2)

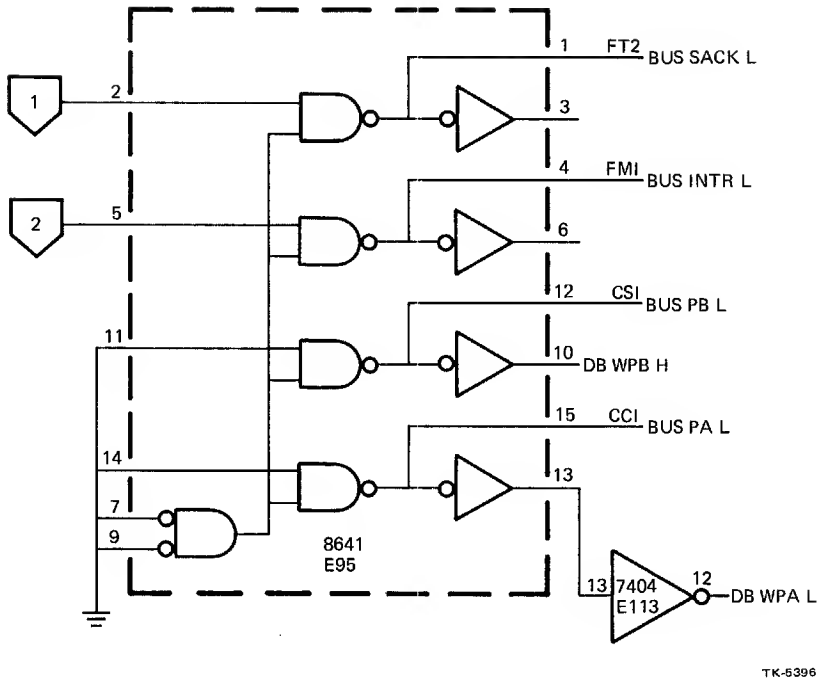

Figure 4-3 Interrupt Logic (Sheet 2 of 2)

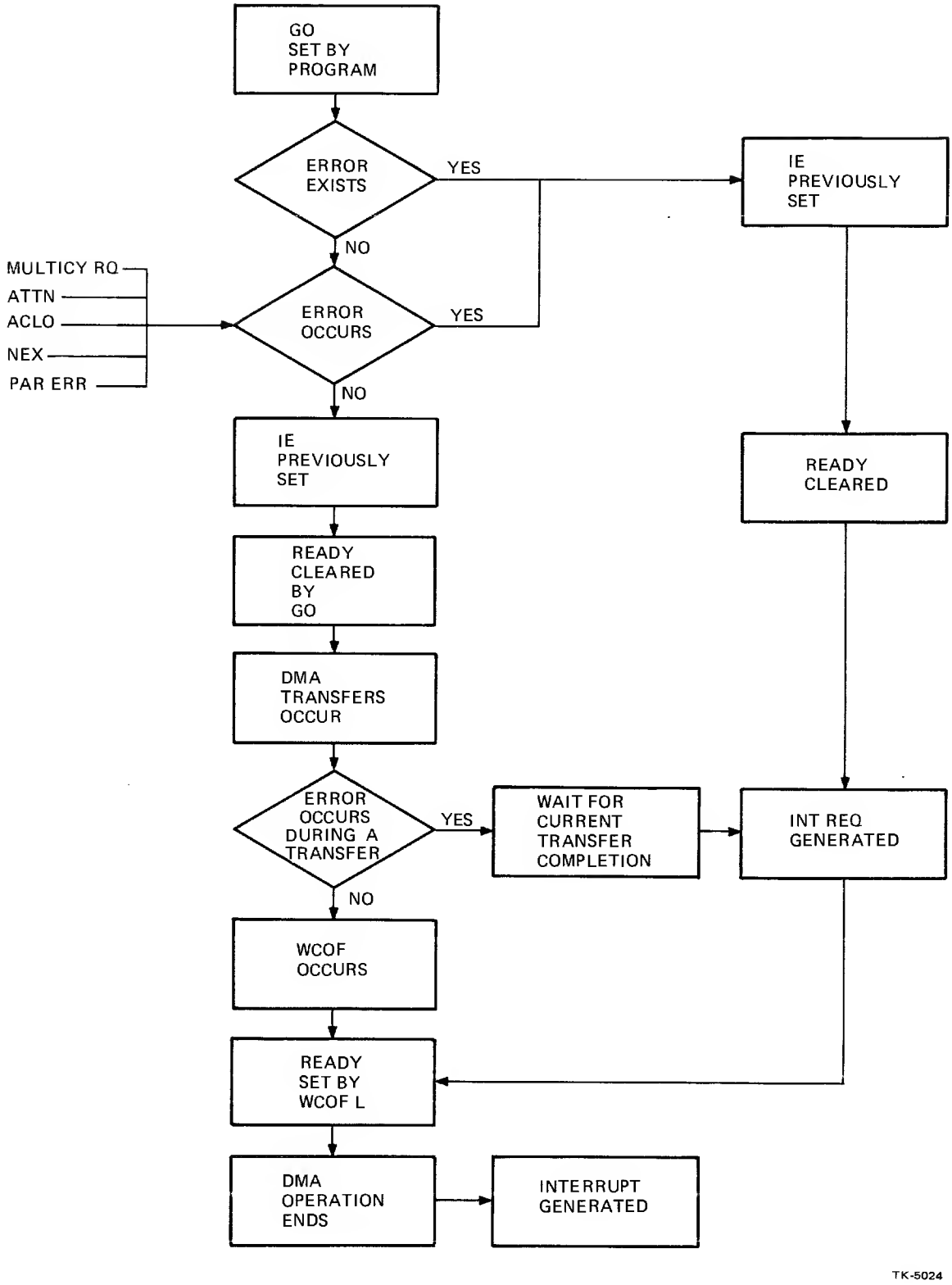

Figure 4-4 Interrupt Flow Diagram

The user device generated data is transmitted to the UNIBUS through the input data register (IDR).

DMA operation begins when the DR11-W sends GO L and READY L to the user device. These signals are generated in the control logic, within which the READY flip-flop is cleared by a GO pulse if no ERROR condition exists. The BUSY flip-flop in the control logic is cleared by CPU initialization (BUS INIT L) or by completion of the previous NPR operation.

To initiate a DMA operation, the user device checks BUSY L to determine whether or not the DR11-W is in a busy cycle. If BUSY L is not asserted (i.e., the DR11-W is not busy), the user device can initiate a transfer.

Fifty ns after the delay line is triggered via MCYCLE RQ H, the burst DLT multivibrator in the control logic is turned on, and the NPR RQ flip-flop is set. Setting this flip-flop clocks BURST RQ L if the user device has requested a burst transfer. Receipt of NPR RQ by the bus master logic asserts BUS NPR on the UNIBUS while simultaneously inhibiting the interrupt logic from generating BUS INTR L. NPR RQ also prevents the control logic from generating an ERROR L output that could also cause an interrupt.

150 ns after the control logic delay line is triggered by the CYCLE RQ (A or B) input, WCLK H is sent to the word count register (WCR). WC CLK H increments the WCR. If the final transfer is in progress, the WCR generates WCOF L, which sets the control logic READY flip-flop.

200 ns after the control logic delay line is triggered, the CY INH flip-flop is set. Flip-flop output then inhibits further triggering of the delay line and resets the CYCLE flip-flop.

At 400 ns after the control logic delay line is triggered, C0 RST clears BUSY. The DR11-W BUSY output then goes high, enabling the user device to execute another transfer request. The user device can then send a second CYCLE RQ (A or B), together with appropriate data and control signals, even though the preceding transfer is still in progress.

If a second CYCLE RQ is made while BUSY is asserted, the MULTICYCLE flip-flop in the control logic is set, and in turn, sets ERROR. Upon completion of the first data transfer, the control logic CY INH flip-flop is cleared. The delay line is then no longer inhibited, and a second data word can be transferred.

CHAPTER 5
INTERFACING AND PROGRAMMING CONSIDERATIONS

5.1 USER-DEVICE CABLES

Two identical cable/connector assemblies are required for interfacing the DR11-W with a user device. The recommended BC06R cable assembly is terminated at both ends with H855 40-pin female connectors that mate with the J1 (output) and J2 (input) connectors of the DR11-W. The use of cables longer than 1524 cm (50 ft) BC06R is not recommended. If a longer cable is used, satisfactory DR11-W performance cannot be quaranteed. Note that the recommended BC06R cable assemblies are optional equipment items.

5.2 USER-DEVICE SIGNAL INTERFACE

The DR11-W uses 8881 I/O signal drivers and 8640 receivers, both of which terminate into a 120-ohm impedance. It is recommended that the 8881 and 8640 also be used in the user device. They may be purchased from DIGITAL by specifying DIGITAL part numbers 957 and 956, respectively.

NOTE

User I/O receivers and drivers should be grounded, capacitor by-passed, and physically positioned within 10.2 cm (4 in) of the inboard end of the module "fingers."

5.3 I/O SIGNAL TIMING

User device operation with the DR11-W may be initiated any time after the READY and BUSY signals to the user device are cleared; clearing indicates that the DR11-W is ready for DMA operation. READY is cleared by the GO pulse; BUSY is cleared during initialization or on completion of a previous cycle.

After READY and BUSY are cleared, the user device may initiate data and control signals for the DR11-W. When the user device has data ready for transfer, the following group of signals must be asserted simultaneously, and as discrete pulses or signal levels:

DI (15:00) H
CYCLE RQ (A OR B)/BURST RQ L*
C0 CNTH H; C1 CNTL H†
A00 H
WC INC ENB H
BA INC ENB H

*Either or both of these signals are asserted, depending upon transfer conditions.

†These signals are always used together as a 2-bit code (see the functional description of DR11-W input signals in Table 3-1).

CYCLE RQ A (or B) must be held for 120 ns after assertion; the data and other control signals in the listed group must be held for 250 ns after assertion. BURST RQ L, however, must be held until the entire string of transfers is completed. Note that the burst request signal is the only DR11-W I/O signal asserted low at any time.

NOTE

The DR11-W automatically compensates for skew times introduced by drivers, receivers, or interconnect cables.

The user device data and control signals to the DR11-W are buffered by the IDR and the ICR, respectively. During a DATO/B cycle, new user data and control signals may be sent to the DR11-W upon receipt of the trailing edge of the low-to-high BUSY signal if READY is still cleared. Similarly, the leading edge of the BUSY pulse may be used to strobe the contents of the ODR into the ODR drivers during the DATI/P cycle.

If another CYCLE RQ A (or B) H is received while a bus cycle is in progress, a MULTICY RQ fault signal is generated in the DR11-W. If an IE has already been generated in the DR11-W control logic, MULTICY RQ H causes an interrupt request to be generated at the completion of the current cycle.

When data is transferred in burst mode, each cycle cannot exceed the limit established by the data late timeout setting (adjustable from 4 to 40 usec, maximum, and 10 to 15 usec nominal). If this timeout limit is exceeded, the bus is automatically released, and must be regained by means of the established bus request/bus grant sequence before another data transfer can be effected.

5.4 SIGNAL INTEGRITY

The DR11-W is designed to perform as a DMA interface for user devices located in the same enclosure as the DR11 itself. For this type of application, an enclosure is defined as a mounting framework consisting of one or more cabinets bolted together to form a complete assembly. The electrical bonding within the enclosure is expected to be adequate for assuring a uniform electrical reference for both the DR11-W and the user device.

NOTE

The interface circuits used in the DR11-W are single-ended (not differential), and therefore must operate in an environment that provides the same reference at both ends of the interconnecting cable. Furthermore, it is unwise to dress cables outside of the enclosure unless they are designed for this purpose. Failure to observe these recommendations can result in increased system sensitivity to environmental noise and consequent reduction in system reliability.

The interface circuits of the DR11-W are designed for optimized signal-to-noise margin. They feature current drive, threshold control, and input/output impedance characteristics that enhance the reliability of the DR11-W/user interface. The same circuits must be designed into the user device if the full value of the designed-in noise immunity is to be realized in the system operation. The recommended circuits are illustrated in Figure 5-1.

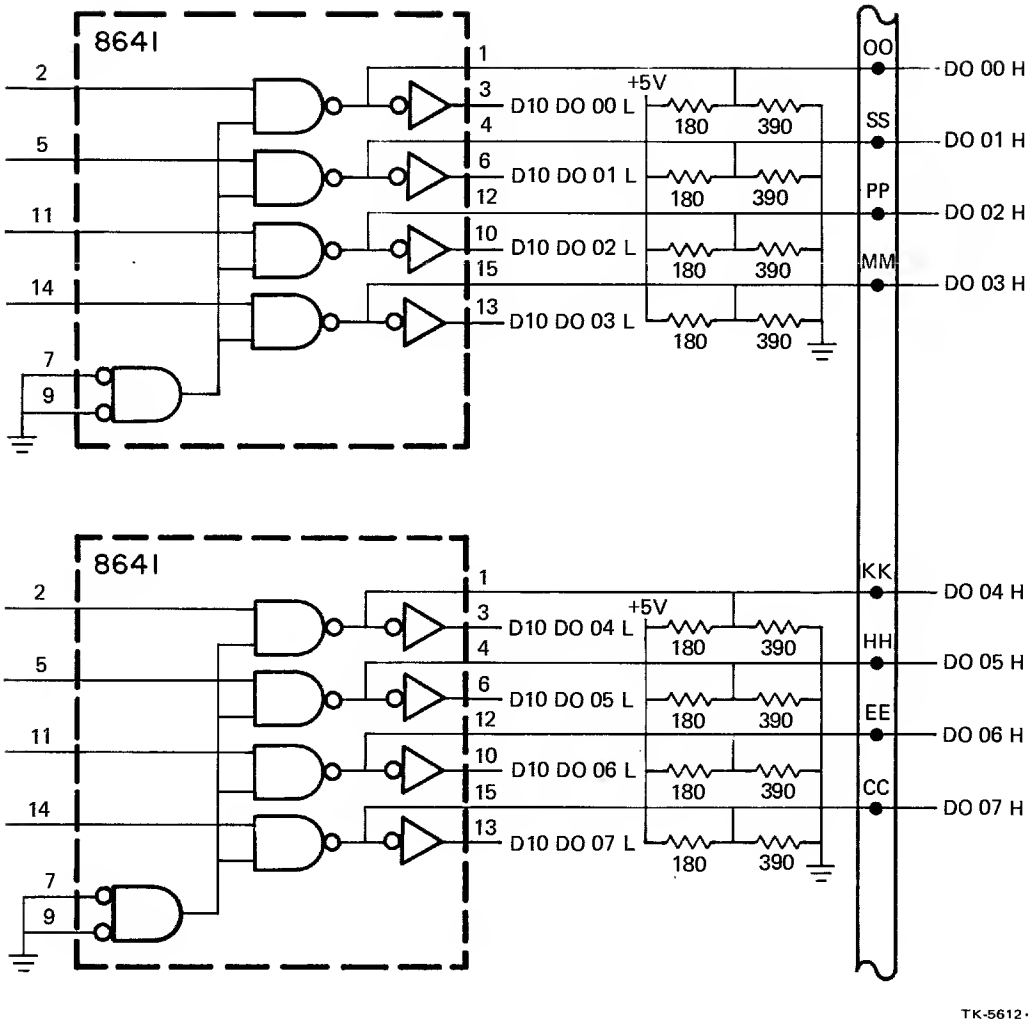

Figure 5-1 Interface Circuits for Optimizing DR11-W Signal-to-Noise Margin

5.5 PROGRAMMING CONSIDERATIONS

Individual consideration of programming requirements may be necessary in connection with:

- DR11-W operating mode
- Cable length, and
- Timing relationships.

5.5.1 DR11-W Mode

In general, read/modify/write (R/M/W) instructions should not be used when addressing the CSR in DR11-W mode operation. This restriction is necessary because, when writing, bits 15 and 0 have different meanings than when reading. This difference is due to the presence of the EIR in the DR11-W mode, a consideration that does not apply when operation is in the DR11-B mode.

5.5.2 Timing

The user device must have sufficient time to receive and decode the function bits prior to executing commands. To meet this requirement, either the software or the user hardware must delay GO long enough to allow cable deskew and function decode. The software may deskew, by first setting the function bits (Figure 5-2), then asserting both the function and GO bits. This provision allows at least one instruction time for the function bits to be propagated and decoded.

In a link situation, if FNCT 2 was asserted (thereby interrupting the responding processor), the FNCT 2 bit should be cleared after the GO bit has been set, as shown in Figure 5-2.

5.5.3 Programming Example

The following programming examples for the PDP-11 and VAX applications for the DR11-W illustrate the two concepts outlined in Paragraph 5.5.2. Note that an R/M/W has been used in the interrupt service code. BIS (an R/M/W instruction) is a usable (and, in fact, desirable) instruction in this case because bit 15 is going to be set regardless of its present state. (Bit 15 is the bit that might accidentally be modified by an R/M/W.) The example also uses the byte form of instruction (BISB) to avoid any interaction with the GO bit contained in the low byte.

Example 5-1 gives a typical VMS coding sequence for loading the CSR in a DR11-W/VAX system configuration. Example 5-2 gives the coding sequence for reading the CSR after interrupt in this configuration. Examples 5-3 and 5-4 give a similar pair of examples for a VAX/PDP-11 system configuration.

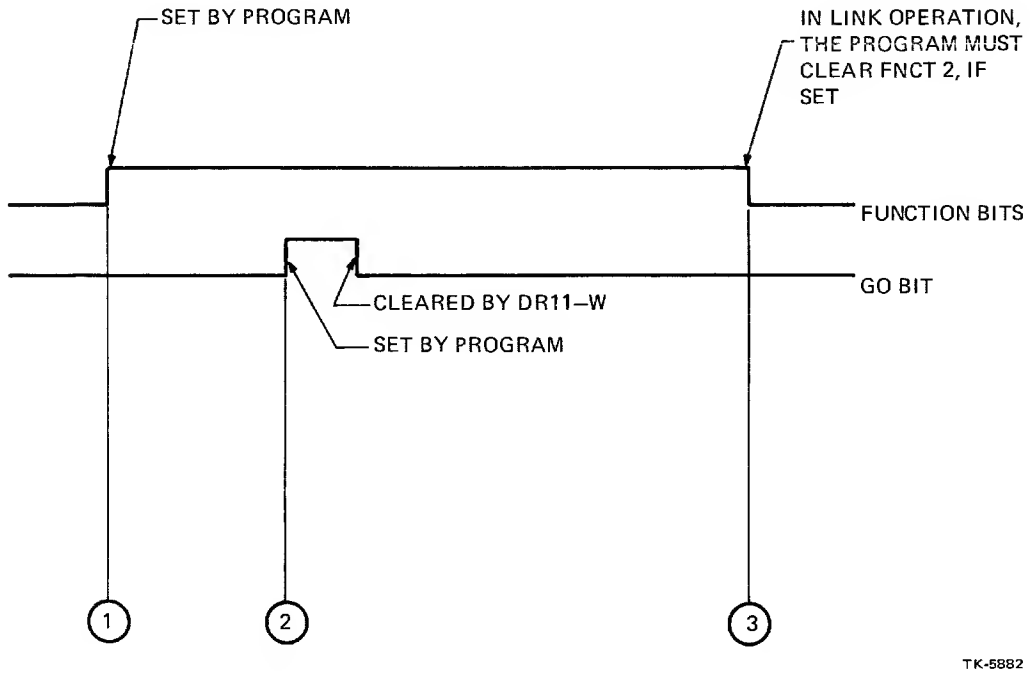

Figure 5-2 Setting and Clearing FNCT2 and GO Bits

```
; INPUTS:
;
;       TRANSFER_COUNT - Address of location containing negative ;
;                        number of words to transfer.
;       BUS_ADDRESS - Address of location containing low 16 bits
;                     of Unibus address of data buffer.
;       CSR_CONTENTS -   Address of location containing value to
;                        load into DR11-W CSR.
;
;                        Includes:
;                                1) Go bit (bit Ø)
;                                2) Functions bits (bits 3:1)
;                                3) Extended bus address bits
;                                   (bits 5:4)
;                                4) Interrupt enable bit (bit 6)
;
;       R4 - Contains address of DR11-W register set.
;
;  FUNCTIONAL DESCRIPTION:
;
;       This routine loads the specified values in the DR11-W
;       registers to start a transfer.  In the case of the CSR,
;       its contents are written first to the CSR less the "GO"
;       bit since the "FUNCTION BITS" must be allowed to
;       stabilize.  Next the CSR is written with all values,
;       including the "GO" bit to actually start the transfer.
;       Finally, the CSR is written less the "GO" bit (so this bit
;       isn't set twice) and less "FUNCTION BIT" 2.  This last   ;
;       step is optional,  depending on whether the DR11-W is used
;       in LINK MODE.


        MOVW    W^TRANSFER_COUNT,(R4)    ; Load the transfer count
                                           register
        MOVW    W^BUS_ADDRESS,2(R4)      ; Load low 16 bits of bus
                                           address
  1. BICW3  #1, W^CSR.CONTENTS,4(R4); Load CSR less "GO" bit
  2. MOVW   W^CSR.CONTENTS,4(R4)     ; Load CSR, assert "GO"
  3. BICW3  #5,W^CSR_CONTENTS,4(R4) ; Load CSR less "GO" and
                                      "FNCT" bit 2
                                    ; This final step is for
                                      LINK operation only.
```

Example 5-1 Typical VMS Coding Sequence for Loading the CSR in a DR11-W/VAX System Configuration

```
;++
; Coding sequence for reading DR11-W CSR after interrupt
;
; INPUTS:
;
;       R4 - Address of DR11-W register set
;
; OUTPUTS:
;
;       DR.BAR - Final contents of DR11-W Bus Address Register
;       DR.WCR - Final contents of DR11-W Word Count Register
;       DR.IDR - Final contents of DR11-W Input Data Register
;       DR.CSR - Final contents of DR11-W Control and Status
;                Register
;       DR.EIR - Final contents of DR11-W Error Information
;                Register


;--     MOVW     4(R4),W^DR.CSR      ;  Read Control and Status
                                     ;  Register
       BISB     #128,5(R4)          ;  Set EIR flag
       MOVW     4(R4),W^DR.EIR      ;  Read Error Information
                                     ;  Register
       BICW3    #^C<14>,W^DR.CSR,
                4(R4)               ;  Write CSR, clearing all
                                     ;  status except FNCT bits
       MOVW     (R4),W^DR.WCR       ;  Save Word Count Register
       MOVW     2(R4),W^DR.BAR      ;  Save Bus Address Register
       MOVW     6(R4),W^DR.IDR      ;  Save Input Data Register
```

Example 5-2 Typical VMS Coding Sequence for Reading the DR11-W CSR After Interrupt in the DR11-W/VAX System Configuration

```
;       INPUTS:
;
;       TRANSFER_COUNT - Address of location containing negative
;                        number of words to transfer.
;       BUS_ADDRESS - Address of location containing low 16 bits
;                        of Unibus address of data buffer.
;       CSR_CONTENTS - Address of location containing value to
;                        load into DR11-W CSR.
;
;                        Includes:
;                                1) Go bit (bit Ø)
;                                2) Function bits (bits 3:1)
;                                3) Extended bus address bits
;                                   (bits 5:4)
;                                4) Interrupt enable bit (bit 6)
;
;       R4 - Contains address of DR11-W register set.
;
; FUNCTIONAL DESCRIPTION:
;
;       This routine loads the specified values in the DR11-W
;       registers to start a transfer.  In the case of the CSR,
;       its contents are written first to the CSR less the "GO"
;       bit since the "FUNCTION BITS" must be allowed to
;       stabilize.  Next the CSR is written with all values,
;       including the "GO" bit to actually start the transfer.
;       Finally, the CSR is written less the "GO" bit (so this bit
;       isn't set twice) and less "FUNCTION BIT" 2.  This last ;
;       step is optional, depending on whether the DR11-W is used
;       in LINK MODE.
;--

        MOV     TRANSFER_COUNT,(R4)     ; Load the transfer count
                                          register
        MOV     BUS_ADDRESS,2(R4)       ; Load low 16 bits of bus
                                          address
        MOV     CSR.CONTENTS,RØ         ; Fetch CSR value
        MOV     RØ,R1                   ; Copy CSR value
        BIC     #1,R1                   ; Clear "GO" bit
        MOV     R1,4(R4)                ; Load CSR value less "GO"
        MOV     RØ,4(R4)                ; Load CSR, assert "GO"
        BIC     #5,RØ                   ; Clear "GO" and "FNCT" bit
                                        ; 2
        MOV     RØ,4(R4)                ;  Load CSR less "GO" and
                                        ; "FNCT" bit 2
                                        ; This final step is for
                                        ; LINK operation only.
```

Example 5-3 Typical Coding Sequence for Loading the DR11-W CSR in a DR11-W/PDP-11 System Configuration

```
;
; INPUTS:
;
;       R4 - Address of DR11-W register set
;
; OUTPUTS:
;
;       DR.BAR - Final contents of DR11-W Bus Address Register
;       DR.WCR - Final contents of DR11-W Word Count Register
;       DR.IDR - Final contents of DR11-W Input Data Register
;       DR.CSR - Final contents of DR11-W Control and Status
        Register
;       DR.EIR - Final contents of DR11-W Error Information
        Register
;__
        MOV     4(R4),R0        ; Read Control and Status Register
        MOV     R0,DR.CSR       ; Save CSR contents
        BISB    #200,5(R4)      ; Set EIR flag
        MOV     4(R4),DR.EIR    ; Read Error Information Register
        BIC     #^C<16>,R0      ; Clear all status except "FNCT" bits
        MOV     R0,4(R4)        ; Write CSR, clearing status bits
        MOV     (R4),DR.WCR     ; Save Word Count Register
        MOV     2(R4),DR.BAR    ; Save Bus Address Register
        MOV     6(R4),DR.IDR    ; Save Input Data Register
```

Example 5-4 Typical Coding Sequence for Reading the CSR After Interrupt in the DR11-W/PDP-11 System Configuration

CHAPTER 6
INSTALLATION

6.1 UNPACKING AND INSPECTION

6.1.1 Unpacking

To unpack the DR11-W, perform the following procedure:

1. Check that the shipping container is sealed.

2. Check the shipment against the packing list to ensure that the correct number of containers has been received. If the shipment is incorrect, notify DIGITAL.

NOTE

The customer should first check with the carrier to try to locate the missing item(s).

3. Check all containers for external damage. If any damage is found, notify DIGITAL.

4. Open containers one at a time. If there is more than one, start with the container labeled "Open Me First." Inventory the contents of each package by comparing it with its packing slip.

NOTE

Packing materials such as foam fillers and plastic inserts should be retained if reshipment is a possibility.

6.1.2 Inspection

Inspect each component for damage, e.g., scratches or breaks. Report any damage to DIGITAL.

6.2 INSTALLATION PROCEDURE

To install the DR11-W, carry out the following procedure:

1. Ascertain that the system +5 V power supply can handle the additional load (3.7 A) presented by the DR11-W.

2. See that the system power is OFF.

3. Remove the grant continuity card (G727A) from the backplane SPC slot in which the M8716 DR11-W module is to be installed.

4. Remove the NPG jumper from the slot to be occupied by the DR11-W module. This jumper is a backplane wire connecting pins CA1 and CB1.

5. If the DR11-W is to be operated at a BR level other than BR5, the standard BR5 plug (PN 54-8778) illustrated in Figure 6-1 should be replaced with the appropriate plug (see Table 6-1).

6. Set the bus address by means of switchpack E120 (Figure 6-2) and in accordance with the switch settings given in Table 6-2. The switchpacks used in the DR11-W are of two types: rocker and slide. The individual switches comprising a switchpack are set to logical 0 by setting them to their ON position as indicated by the OFF-ON lettering at one end of the switch package. For both types of switchpacks, ON represents logical 0; OFF is logical 1. The switchpack with slide-type switches poses no problem in address setting. Each switch lever is merely pushed in the ON or OFF direction (Figure 6-2) to set it for logical 0 or 1, as desired. To set any switch of the rocker type to ON (logical 0), depress the switch at its ON end (do not be concerned with the red bars at each end of the switch lever). Similarly, to set the switch to logical 1, depress the end of the switch at its OFF end.

7. Set the vector address by means of switchpack E15 (Figure 6-2) and in accordance with the switch settings given in Table 6-3. Vector addresses must be assigned from available floating vector space (rank = 42).

8. For link-mode operation, set the switches of operational mode switchpack E105 (Figure 6-3) in accordance with the switch settings in Table 6-4.

9. For diagnostic runs, set burst mode selection switch B1 (Figure 6-4) for 2-cycle or N-cycle operation in burst mode, as desired. The switch position for each mode is etched adjacent to the switch on the module.

NOTE

When the DR11-W is used as the functional equivalent of the DR11-B, switch 5 of operational mode switchpack E105 (Figures 1-1 and 6-3) should be set to OFF, so that BIT SET and BIT CLR instructions can be sent to the DR11-W CSR.

NOTE

When looking at the component side of the M8716 module, the 2-CYC position of switch B1 is toward the operational mode switchpack E105 (Figure 6-4).

10. Install the DR11-W in the backplane.

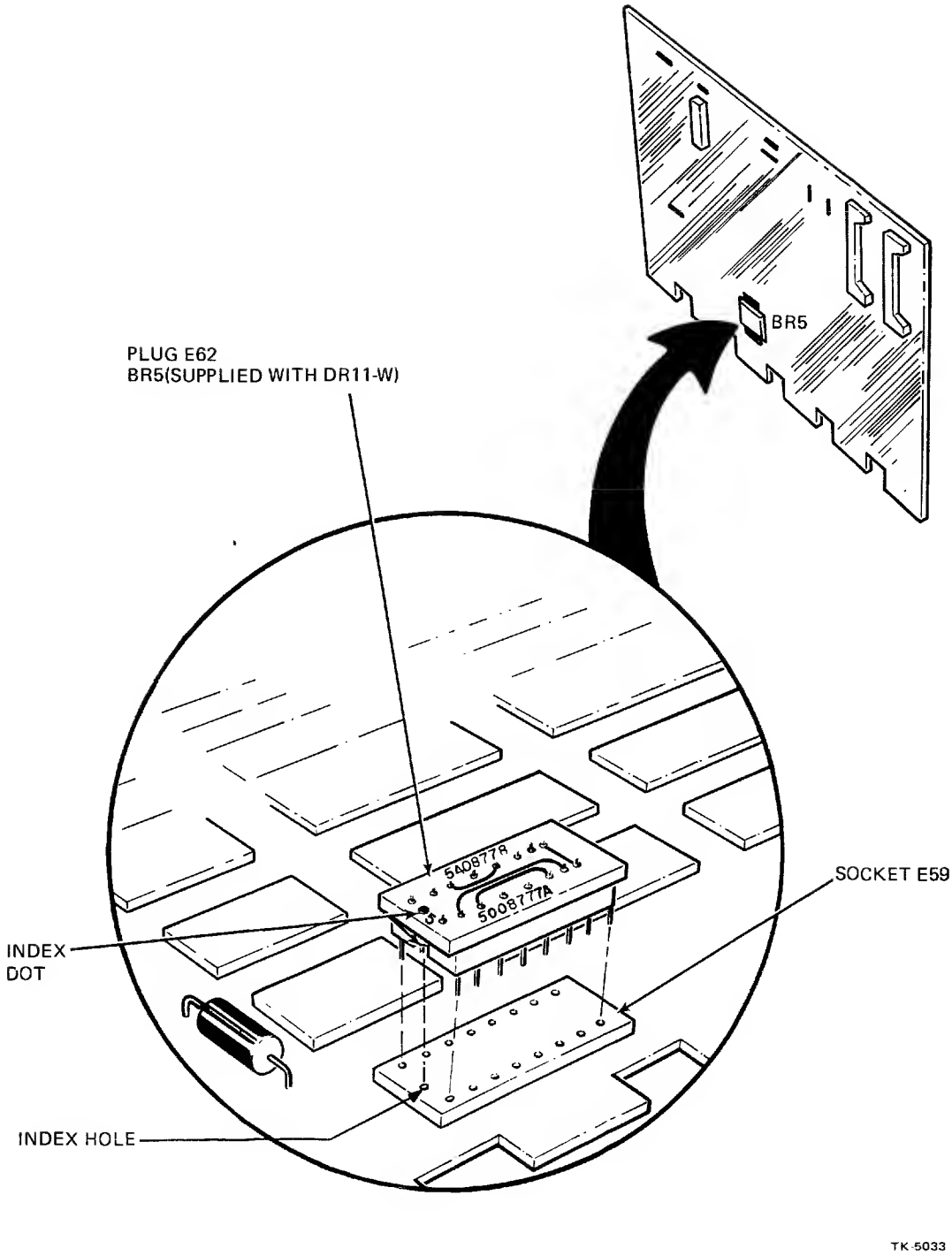

Figure 6-1 Bus-Request, Priority-Level Plug/Socket Assembly

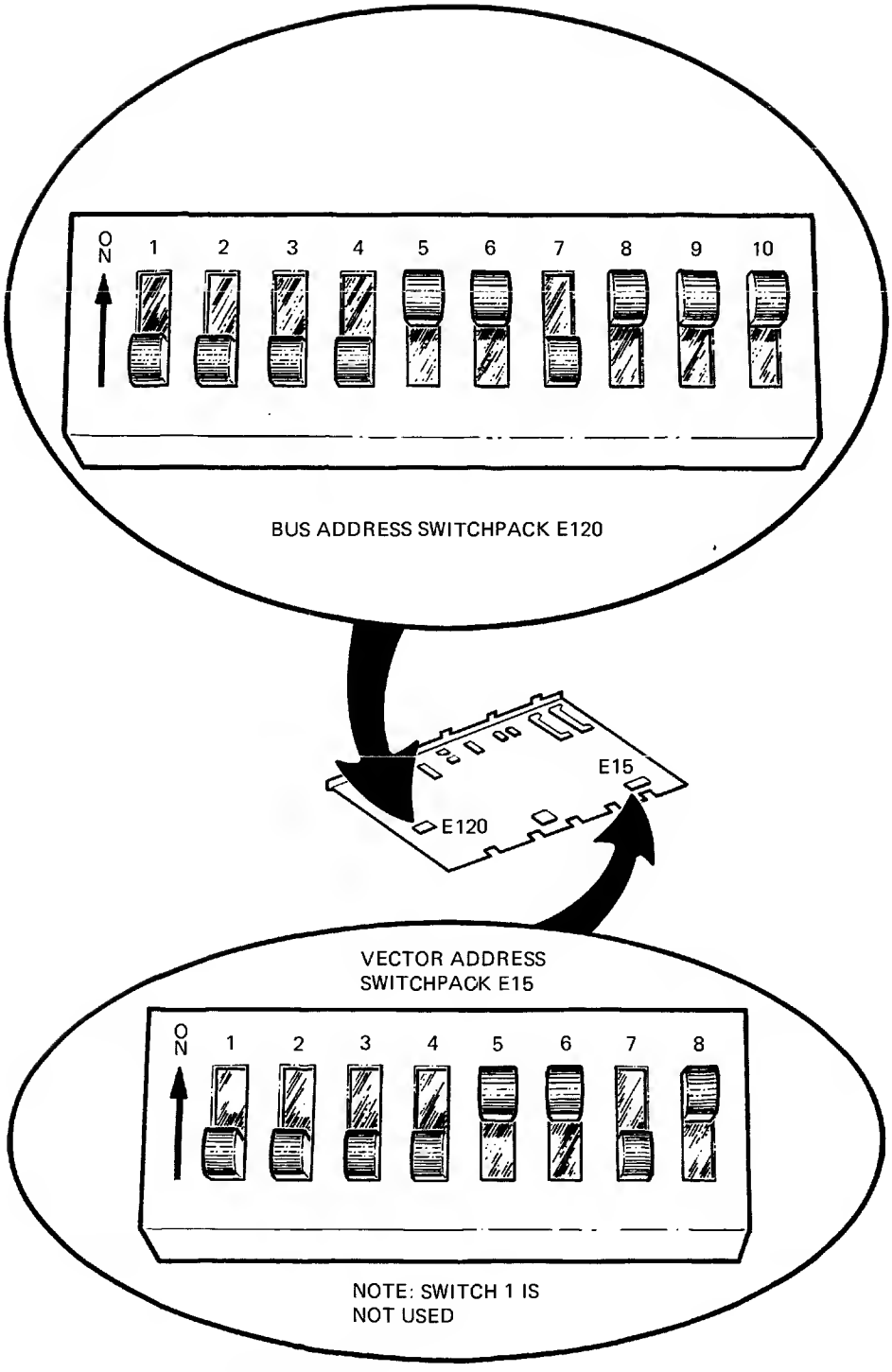

Figure 6-2 Bus Address and Vector Address Switchpacks

Table 6-1 Available Bus-Request Priority-Level Plugs

Priority Level	BR Plug Part Number
BR7	54-8782
BR6	54-8780
BR5	54-8778
BR4	54-8776

Table 6-2 Typical Switch Settings for Bus-Address Switchpack E120

Bus Address Bits BA(12:03)	12	11	10	9	8	7	6	5	4	3
Switch Number	1	2	3	4	5	6	7	8	9	10
Typical Switch Settings for:										
DR11-W Module #1 (77241X)	OFF	ON	OFF	ON	OFF	ON	ON	ON	ON	OFF
DR11-W Module #2 (77243X)	OFF	ON	OFF	ON	OFF	ON	ON	ON	OFF	OFF
DR11-W Module #3 (77245X)	OFF	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF
DR11-W MODULE #4 (77247X)	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF

Notes:

1. A switch is set to OFF for logical 1, and to ON for logical 0.
2. X is used for the register number (0 = WCR; 2 = BAR; 4 = CSR/EIR; 6 = IDR/ODR).
3. The user may employ additional DR11-Ws if he wants; these are set to addresses in user floating address space.
4. For floating addresses, the CSR address is rank 19.

Table 6-3 Switch Settings for Vector Address Switchpack E15

Vector Address Bit		1	2	3	4	5	6	7	8
Switch Number		1	2	3	4	5	6	7	8
Switch Setting*									
124_8	X	OFF	ON	OFF	ON	OFF	ON	ON	
300_8	X	ON	ON	ON	ON	OFF	OFF	ON	

NOTE
Vector address floating = rank 42

*Settings in this example are for octal address 124

Legend: X = Don't care
ON = Logical 0
OFF = Logical 1

Table 6-4 Switch Settings for Operational Mode Switchpack E105

Switch Number	1	2	3	4*	5†
Name	BUSY	BUSY	CYC INH	READ INH A00	MODE SEL
User Device	ON	OFF	OFF	USER SEL	USER SEL††
Maintenance Cable Mode	OFF	ON	OFF	OFF	USER SEL
DR11-W to DR11-W Link Mode	OFF	ON	OFF	ON	ON
DR11-W to DRV11-B Link Mode	OFF	OFF	ON	ON	ON

*Switch 4 is set to ON for link mode operation to prevent odd addressing when the device uses address line A00; when set to OFF, switch 4 ungrounds the A00 line upon assertion of READY.

†Switch 5 is set to ON to select the DR11-W mode; OFF selects the DR11-B mode. The DR11-B mode provides software compatibility with the DR11-B general purpose interface. The DR11-B mode disables the EIR and allows execution of read-modify-write instructions.

††For VAX systems, only the DR11-W mode (switch set to ON) is supported. For PDP-11 systems, both DR11-W mode (switch set to ON) and DR11-B mode (switch set to OFF) are supported.

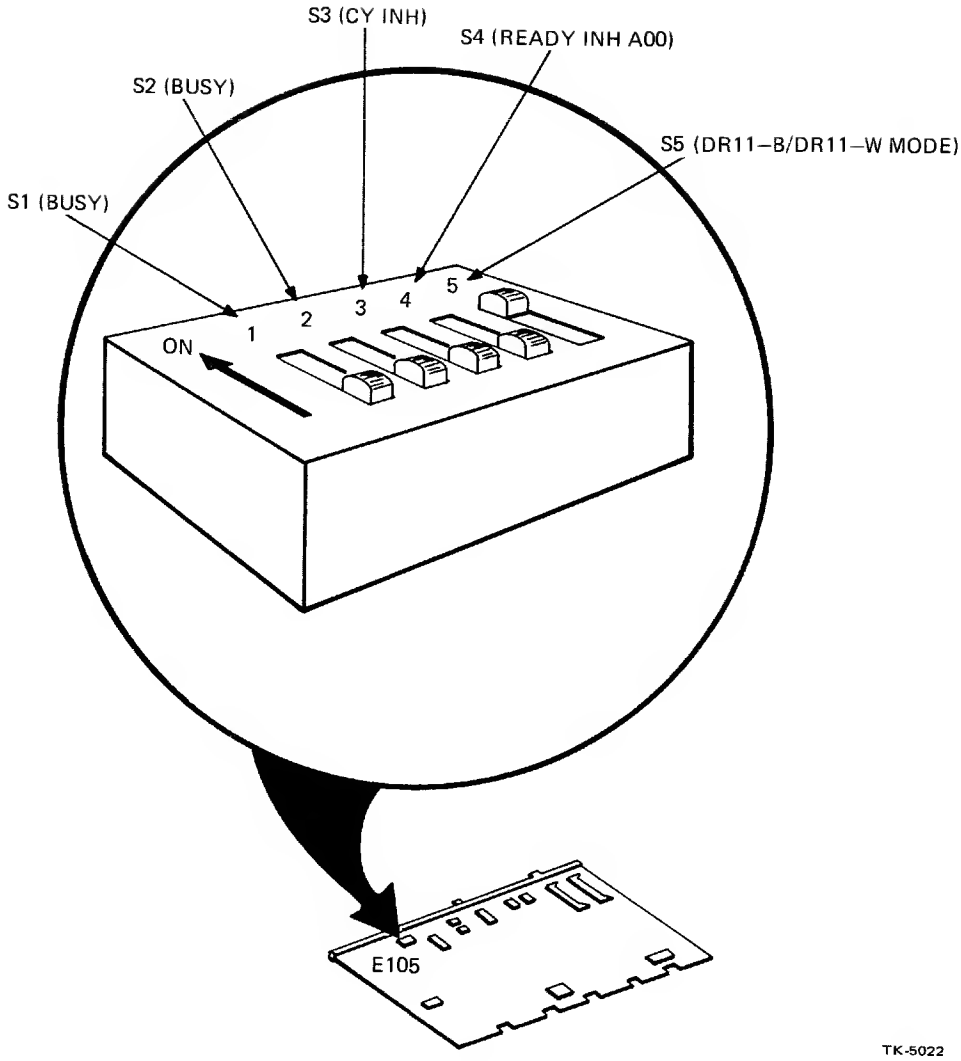

Figure 6-3 Operational Mode Switchpack E105

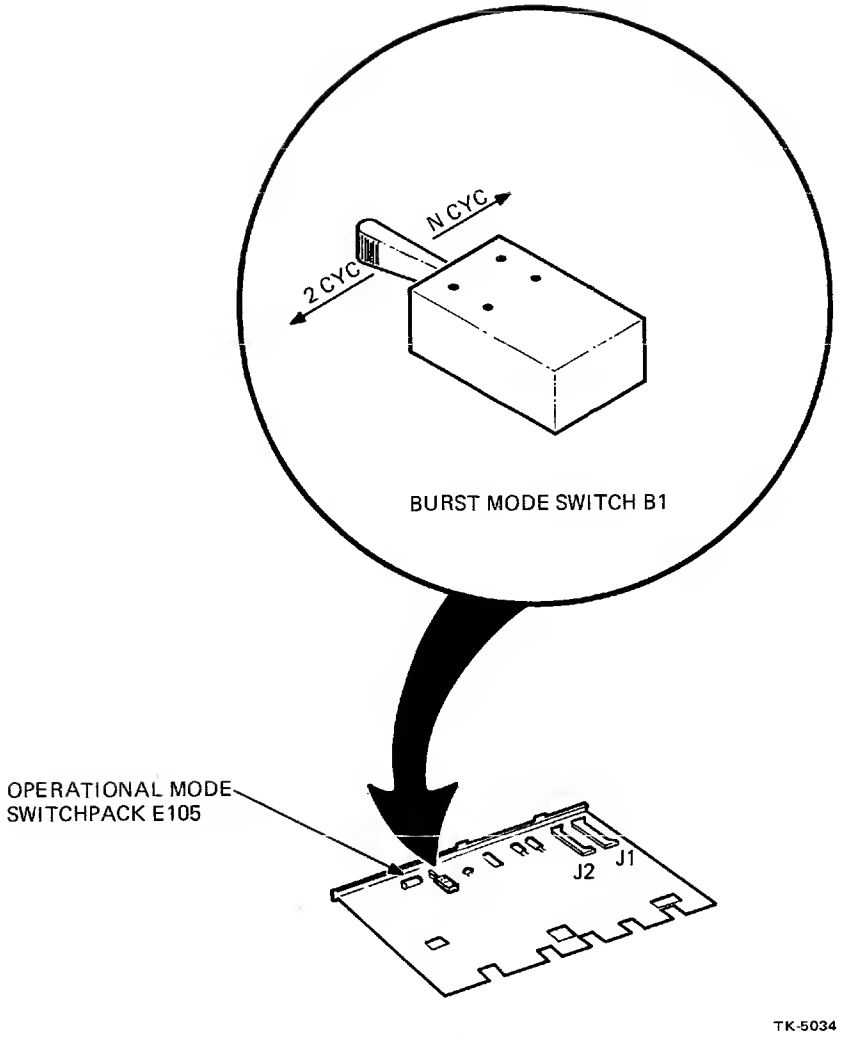

Figure 6-4 Burst Mode Switch B1

6.3 ACCEPTANCE TESTING

Acceptance testing of the DR11-W is performed by running the appropriate diagnostic program for the DR11-W system configuration under test. Refer to Chapter 8 of this manual for the DR11-W diagnostic programs provided. To run the program, perform the following procedure:

1. Connect the wraparound test cable BC05L between output connector J1 and input connector J2 on the DR11-W (Figure 1-1).

2. Connect an oscilloscope probe to test point TP1 on the DR11-W.

3. Turn on system power.

4. Start diagnostic run.

5. Upon instruction from diagnostic, calibrate BURST DLT TO (burst data late timout) for 12 usec (typical)* by adjusting potentiometer R80 (Figure 1-1), and the oscilloscope connected in step 2.

6. Run remaining portion of diagnostic applicable to the system configuration under test.

NOTE

For PDP-11 installations, a single program is run straight through. For VAX-11/UBA installations, the maintenance wrap/cable wrap diagnostic is run for fault detection only; a second (stand-alone) diagnostic is run to support detailed testing of the DR11-W at the hardware level. Refer to Chapter 8 for further details.

7. Remove the BC05L maintenance/wraparound cable connecting J1 and J2.

8. Connect the two BC06R cables (Figure 1-1) to J1 and J2, respectively, and to the user device.

9. If the DR11-W has passed the above tests, proceed with system operation.

CAUTION

Prior to starting diagnostic testing, ensure that the user device has been powered down, and that the two BC06R cables for DR11-W user device interconnect have been unplugged.

*Or for whatever time is appropriate to the user device.

CHAPTER 7
INTERPROCESSOR LINKS

7.1 GENERAL

The DR11-W can be configured for operation as a DMA parallel-data transfer link between two computer systems (Figures 1-3 and 7-1). The link operates in a half-duplex communications mode; i.e., it has the capability of transmitting data bidirectionally between the two computer systems, but in only one direction at a time. Link applications require that the DR11-W be set in the DR11-W mode (Table 6-4).

7.2 OPERATING MODES

From a hardware standpoint, the link can operate in either of three modes:

1. Word mode
2. Block mode
3. Burst mode

In word mode, information can be passed between two computers in a word-by-word sequence controlled by an interrupt-driven program. In the block and burst modes (which to the software are essentially identical), the link transmits a contiguous block of memory data from one computer to the other. DMA transfer is used in both machines. The principal difference between the two modes of operation is that in the block mode, the DR11-W must obtain and release the bus for each data transfer made. In the burst mode, the DR11-W holds onto the bus, once the bus grant is received, until the requested 2-cycle or N-cycle transfer is completed.

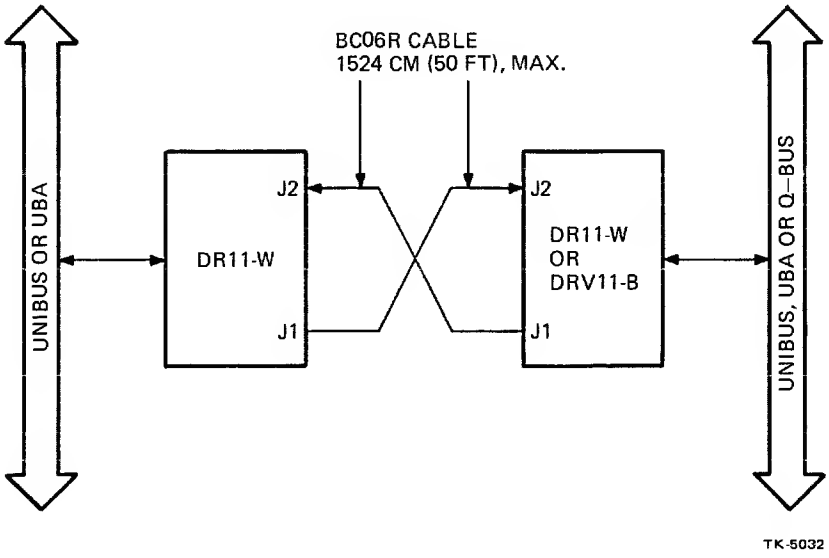

Figure 7-1 Interprocessor Link Block Diagram

Each of the computers in the link configuration maintains independent control of its own interfaee. The programs for the two computers must be written so as to ensure compatibility in terms of information flow direction, setting bus address registers, and control of word count at the respective computer interfaces with the DR11-W.

In the environment provided by the VAX-system software (and recommended for the PDP-11s) the communication between the linked computers is established by means of CSR bits (03:01) and (11:09), respectively (see Figure 2-1 and Table 2-1 for this register). When CSR bits (03:01) are loaded into the CSR of one DR11-W, the information appears in the other DR11-W of the link configuration. Table 7-1 shows the functional correlation of these bit relationships for the DR11-W and DRV11-B interprocessor links.

Table 7-1 Correlation of CSR Function and Status Bits in Interprocessor Link Operation

CSR Bits			
Transfer-Initiating Computer	**Transfer-Responding Computer**	**DR11-W/DRV11-B Function**	**Meaning of CSR Bit Status at Transfer-Initiating Computer**
Bit 3	Bit 11	Block/Burst NPR Transfer	Set – Block NPR transfer Clear – Burst NPR transfer
Bit 2	Bit 10	INTR (Interrupt) Request	Set – Interrupt of responding computer
Bit 1	Bit 9	DATI/DATO	Set – DATO Clear – DATI

7.2.1 Word Mode

Setting CSR bit 2 (FUNC 2) in the transmitting DR11-W sets both CSR bit 10 (STATUS B) and CSR bit 13 (ATTN) in the receiving DR11-W. ATTN generates ERROR, which in turn generates an interrupt if IE is set.

In all three transfer modes, when powerfailure occurs in one computer, an ACLO is transmitted to the other computer, where it sets ATTN and (as described above) causes an interrupt.

During word-mode transfers, the ODR functions as a write-only register for data transmitted to the other computer. The data must be maintained in the ODR until read by the other computer. In general, this operation requires that the receiving computer send back a "hand shaking" signal to indicate that it has read the data and that the transmitting computer can not modify the data in its ODR.

The interrupt capability incorporated in the CSR can be used in conjunction with the ODR to pass information between computers in a word-transfer interrupt sequence (Figure 7-2).

7.2.2 Block Mode

NPR transfers by the link may be requested by either computer, and may flow in either direction. The NPR cycles always occur in pairs: the first cycle is a DATI (read from memory) by the transmitter; the second cycle is a DATO (write into memory) by the receiver. These alternating pairs of cycles repeat until the entire block has been transmitted.

The computer designated as link transmitter sets GO and CYCLE to generate the first NPR cycle. Subsequent NPR cycles are generated by hardware hand-shaking between the DR11-Ws.

The programming sequence used to initiate a block transfer is given in Figure 7-3.

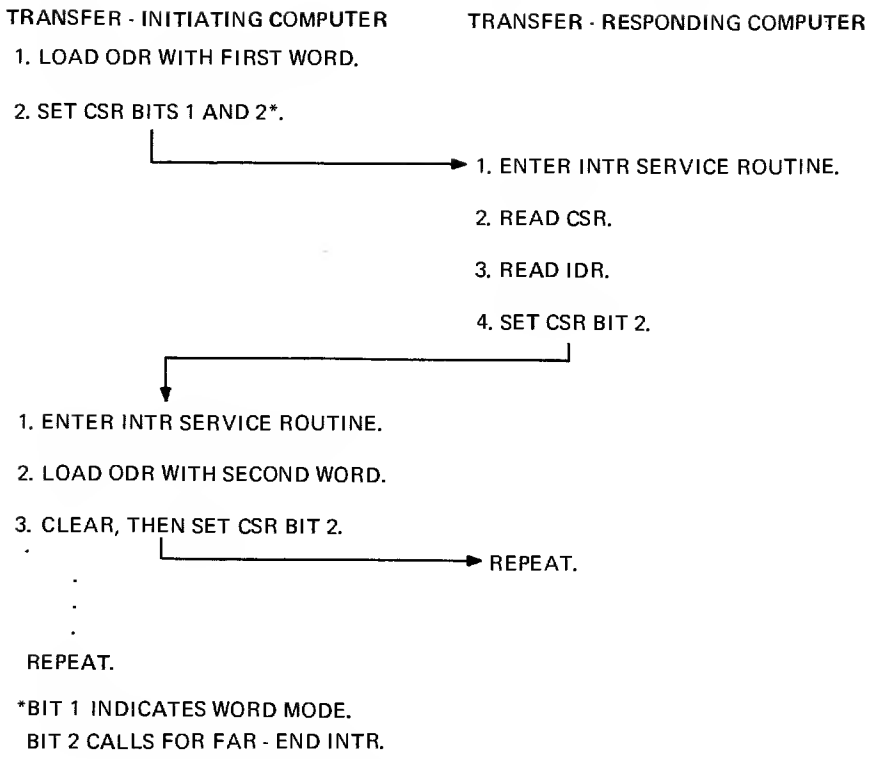

Figure 7-2 Interrupt Sequence for Word Mode Interprocessor Link

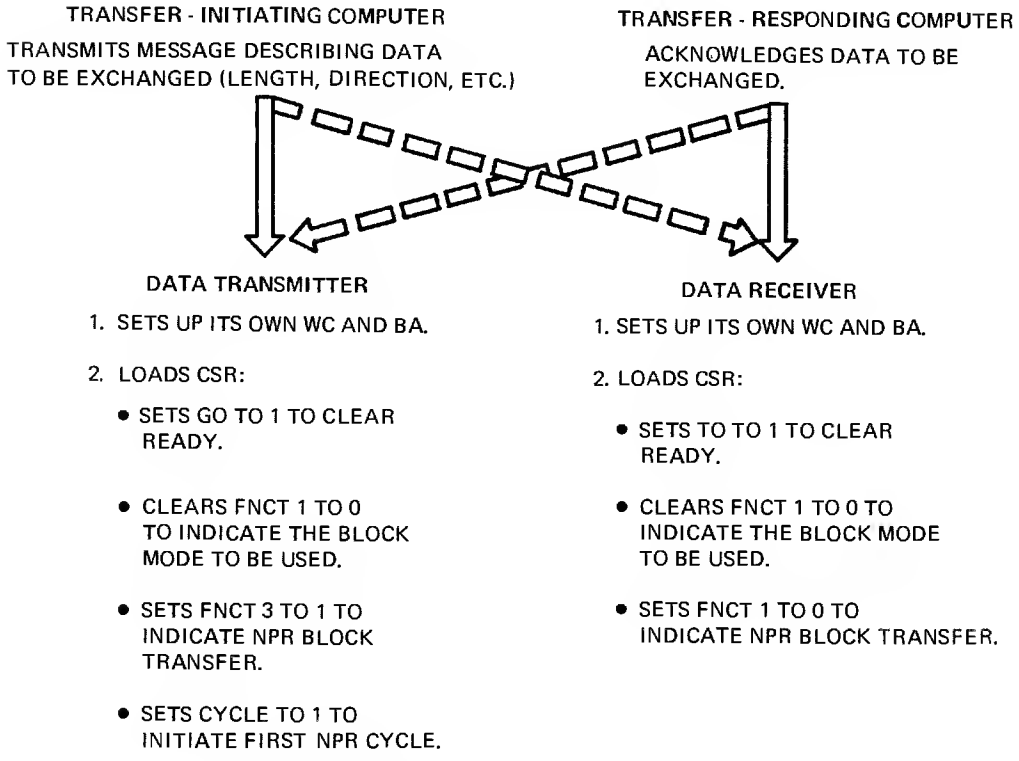

Figure 7-3 Block Transfer Sequence for Interprocessor Link

When the transmitter has read the data word from its memory and loaded the word onto its ODR, BUSY is deasserted. BUSY is connected to CYCLE RQ at the receiving DR11-W. The trailing edge of BUSY triggers an NPR cycle that writes the data word into the receiver's memory. Completion of the write cycle deasserts BUSY in the receiving DR11-W. BUSY returns to the transmitting DR11-W as CYCLE RQ A. This alternating sequence continues until the word count register overflows and halts the block transfer.

NOTE

When the DR11-W forms a link with the DRV11-B, the DR11-W must clear FNCT 3 to 0 while the DRV11-B must set it to a 1, regardless of which computer is the transmitter and which the receiver.

7.2.3 Burst Mode

The NPR burst mode can be operated between two DR11-Ws only, and requires that FNCT 3 be cleared on both DR11-Ws. The programming procedure is similar to the block mode.

Clearing FNCT 3 asserts BURST RQ on the other DR11-W. During the first NPR cycle, the BURST RQ flip-flop sets and stays set until the last NPR cycle, during which WCOF occurs. When the BURST RQ flop is set, it effectively holds the bus from releasing.

The timing of the burst data late one-shot on each DR11-W should be set to accommodate the speed of its companion computer. If one-shot timing is so short as to cause bus drop, link throughput will naturally be degraded.

NOTE

Burst mode cannot be used where a DRV11-B is linked with a DR11-W (see the reference to FNCT bit 3 in the note at the end of paragraph 7.2.2). N-cycle burst mode is not supported in a VAX/DR11-W link.

7.3 PROGRAMMING

The programming characteristics of the interprocessor link are basically the same as those of a single DR11-W configuration. However, when two DR11-Ws are interconnected, the programming of the registers is slightly modified, as explained below.

7.3.1 Word Count Register (WCR)

The function of the WCR is the same as in the nonlink mode. However, the WC INC ENB signal is asserted continually in link mode.

7.3.2 Bus Address Register (BAR)

The basic function of the BAR is unchanged when the DR11-W is operated in link mode. However, since the hardware configuration of the link permanently sets bit 00 to 0, interprocessor transfers are for full words only.

7.3.3 Output Data Register/Input Data Register (ODR/IDR)

The basic function of the ODR/IDR remains unchanged when the DR11-W is operated in link mode.

7.3.4 Control and Status Register (CSR)

In interprocessor link operation, the CSR bits are defined somewhat differently than in link operation. The differences are:

BIT 00 (GO)

When set by itself, GO conditions the DR11-W for either a transmit or a receive transfer.

BITS 1,2,3 (FNCT 1,2,3)

FNCT 1 Is 1 to a receiving DR11-W, and 0 to a transmitting DR11-W. If set in one DR11-W, it is cleared in the other DR11-W. It is initialized by the software.

FNCT 2 Sends an interrupt request to the companion computer; sets STATUS B, ATTN, and READY in the companion computer, thereby causing an interrupt request if the computer's IE bit is set.

FNCT 3 Has two possible meanings:

- In back-to-back DR11-W systems, if FNCT 3 is a 0, the companion computer performs DMA transfers in the burst mode; if FNCT 3 is a 1, the companion computer performs DMA transfers in single-cycle block mode.
- In DR11-W to DRV11-B configurations, FNCT 3 must be written to 0 by the DR11-W. Refer to the note at the end of Paragraph 7.2.2.

BITS 4,5 (XBA 16, 17)

The functions of these bits are the same in both link and nonlink modes. Refer to Table 2-1 for definitions.

BIT 6

The function of this bit is the same in both link and nonlink modes. Refer to Table 2-1 for bit definition. When set, this bit permits the DR11-W to generate an interrupt request if STATUS B sets as a result of FNCT 2 being set in the companion computer.

BIT 7 (READY)

The function of this bit is the same in both link and nonlink modes. Refer to Table 2-1 for bit definition.

BIT 8 (CYCLE)

This bit is used to initiate block and burst transfers when the associated DR11-W is the transmitter. When this bit is set in conjunction with bit 00 (GO), an immediate NPR cycle occurs. The CYCLE bit is also set each time the companion computer requests a bus cycle via CYCLE RQ, and is cleared when the cycle begins.

BITS 9, 10, 11 (STATUS C, B, A)

STATUS C This bit is read by the computer initiating the transfer. If Status C bit is set, the responding computer initiates a DATO; if the bit is cleared, the responding computer initiates a DATI.

STATUS B Reads FNCT 2 of the companion computer. When set, this bit indicates that an interprocessor interrupt has been requested by the companion computer. This bit also sets ATTN and READY, and causes an interrupt request if the IE bit is set.

STATUS A This bit functions somewhat differently in a DR11-W to DR11-W link and a DR11-W and DRV11-B link.

DR11-W to DR11-W Link In this configuration, bit 11 (STATUS A) at 0 indicates a burst mode NPR transfer; if bit 11 is a 1, a block mode NPR transfer is indicated.

DR11-W to DRV11-B Link In this configuration, bit 11 must be set in the DR11-W by the DRV11-B; it must be cleared in the DRV11-B by the DR11-W.

BIT 13 (ATTN)

The function of this bit is the same in the link and nonlink modes. ATTN is also set by either FNCT 2 or ACLO of the companion computer. ATTN generates ERROR. ATTN and ERROR can be cleared by writing 0 to bit 13 of the CSR, or by initialization.

NOTE

ATTN and ERROR cannot be cleared if FNCT 2 of the companion computer is set.

BIT 14

The function of this bit is the same in both link and nonlink modes. Refer to Table 2-1 for bit definition.

BIT 15 (ERROR)

The function of this bit is the same in both link and nonlink modes. Refer to Table 2-1 for bit definition.

7.3.5 Error and Information Register (EIR)

The function of the EIR is the same in both link and nonlink modes. See Table 2-2 for bit definitions.

CHAPTER 8
MAINTENANCE

8.1 GENERAL

For corrective maintenance operations, four diagnostic programs are available for the DR11-W. These programs are:

1. For DR11-W in PDP-11 applications:

CZDRL	Repair-level program (general NPR interface) used in nonlink mode.
CZDRK	Interprocessor exerciser link-mode program.

2. For DR11-W in VAX applications:

ESDRB	On-line (user mode) level 2 program.
ESDRE	Repair-level program for nonlink or link mode.

8.2 ABSTRACTS OF DIAGNOSTIC PROGRAMS

8.2.1 Programs for PDP-11

CZDRL (Nonlink Mode)
This program: (1) is XXDP compatible, (2) permits multiple-board testing by using a table generated by the user, (3) provides for burst data late calibration at a suitable point in the program, and, (4) permits independent use of maintenance wraparound and/or cable wraparound when using the DR11-W in nonlink mode.

CZDRK (Link Mode)
This program provides interprocessor diagnostic testing of the DR11-W and DRV11-B when used in the following link combinations:

PDP-11 UNIBUS/DR11-W	–	PDP-11 UNIBUS/DR11-W
PDP-11 UNIBUS/DR11-W	–	LSI-11 BUS/DRV11-B
PDP-11 UNIBUS/DR11-W	–	VAX UBA/DR11-W
LSI-11 BUS/DRV11-B	–	VAX UBA/DR11-W

For each configuration, the CZDRK (exerciser) program is loaded into each PDP-11. In the two links containing a VAX, the ESDRE program is loaded into the VAX system as described below.

8.2.2 Programs for VAX

ESDRB (Nonlink Mode)

This diagnostic, written in BLISS-32, is for the DR11-W when used with a VAX. The program runs under control of the DIGITAL Diagnostic Supervisor and XA driver to provide an on-line mechanism for determining the logic functionality of the DR11-W by means of a two-part test. The program executes the part or parts specified by the user; i.e., maintenance wrap or (if cable is installed) cable wrap. If neither part is specified, the mainenance-wrap portion is run by itself.

ESDRE (Nonlink or Link Modes)

This repair-level program provides diagnostic support for the DR11-W when used with a VAX in either of two modes; (1) maintenance wrap/cable wrap for nonlink operation and (2) link mode. Since link mode does not support detailed testing of the DR11-W, it is recommended that mode 1 testing be performed prior to link testing. The following link configurations are valid for ESDRE testing:

VAX UBA/DR11-W	–	VAX UBA/DR11-W
VAX UBA/DR11-W	–	PDP-11 UNIBUS/DR11-W
VAX UBA/DR11-W	–	LSI-11 BUS/DRV11-B

When linked to PDP-11s, the PDP-11 should run CZDRK.

APPENDIX A
I/O SIGNAL PIN ASSIGNMENTS

J1

GND	x A	B x	D5 CYCLE RQ A H
GND	x C	D x	D5 ACLO FNCT 2 H
GND	x E	F x	D5 READY H
GND	x H	J x	D5 WC INC ENB H
D5 BURST RQ L	x K	L x	D5 STATUS A H
GND	x M	N x	D5 INIT H
GND	x P	R x	D5 STATUS B H
GND	x S	T x	D5 STATUS C H
GND	x U	V x	D5 STATUS C H
GND	x W	X x	D5 END CYCLE H
GND	x Y	Z x	D5 CYCLE RQ B H
GND	xAA	BBx	GND
D10 DO 07 H	xCC	DDx	D10 DO 08 H
D10 DO 06 H	xEE	FFx	D10 DO 09 H
D10 DO 05 H	xHH	JJx	D10 DO 10 H
D10 DO 04 H	xKK	LLx	D10 DO 11 H
D10 DO 03 H	xMM	NNx	D10 DO 12 H
D10 DO 02 H	xPP	RRx	D10 DO 13 H
D10 DO 01 H	xSS	TTx	D10 DO 14 H
D10 DO 00 H	xUU	VVx	D10 DO 15 H

J2

GND	x A	B x	D5 BUSY H
GND	x C	D x	D5 ATTN H
GND	x E	F x	D5 A00 H
GND	x H	J x	D5 BA INC ENB H
D5 FNCT 3H	x K	L x	D5 FNCT 3 H
GND	x M	N x	D5 C0 CNTL H
GND	x P	R x	D5 FNCT 2 H
GND	x S	T x	D5 C1 CNTL H
GND	x U	V x	D5 FNCT 1 H
GND	x W	X x	D5 GO H
GND	x Y	Z x	GND
GND	xAA	BBx	GND
D4 DI 07 H	xCC	DDx	D4 DI 08 H
D4 DI 06 H	xEE	FFx	D4 DI 09 H
D4 DI 05 H	xHH	JJx	D4 DI 10 H
D4 DI 04 H	xKK	LLx	D4 DI 11 H
D4 DI 03 H	xMM	NNx	D4 DI 12 H
D4 DI 02 H	xPP	RRx	D4 DI 13 H
D4 DI 01 H	xSS	TTx	D4 DI 14 H
D4 DI 00 H	xUU	VVx	D4 DI 15 H

APPENDIX B
SIGNAL CROSS-REFERENCE
DR11-B DR11-W

Table B-1 Signal Cross-Reference DR11-B DR11-W

SLOT C

DR11-B			DR11-W	
PIN	**SIGNAL**		**PIN**	**SIGNAL**
A1	CYCLE REQUEST A H	J1	B	CYCLE RQ A H
A2	+5			
B1	END CYCLE OUT H	J1	X	END CYCLE H
B2	GND	J1	A-C	GND
C1	DAT00 IN H	J2	UU	DI 00 H
C2	GND	J1	E-H	GND
D1	DAT01 IN H	J1	SS	DI 01 H
D2	DAT02 IN H	J1	PP	DI 02 H
E1	DAT03 IN H	J1	MM	DI 03 H
E2	DAT04 IN H	J1	KK	DI 04 H
F1	DAT05 IN H	J1	HH	DI 05 H
F2	DAT06 IN H	J1	EE	DI 06 H
H1	DAT07 IN H	J1	CC	DI 07 H
H2	DAT08 IN H	J1	DD	DI 08 H
J1	DAT09 IN H	J1	FF	DI 09 H
J2	DAT10 IN H	J1	JJ	DI 10 H
K1	DAT11 IN H	J1	LL	DI 11 H
K2	DAT12 IN H	J1	NN	DI 12 H
L1	DSTAT B H	J1	R	STATUS B H
L2	DAT13 IN H	J1	RR	DI 13 H
M1	ATTN H	J2	D	ATTN H
M2	DAT14 IN H	J1	TT	DI 14 H
N1	GND	J1	M-P	GND
N2	DAT15 IN H	J1	VV	DI 15 H
P1	GND	J1	S-U	GND
P2	DSTAT A H	J1	L	STATUS A H
R1	NO LOCK H			
R2	DSTAT C H	J1	T-V	STATUS C H
S1	GND	J1	W-Y	GND
S2	BUSY H	J2	B	BUSY H
T1	GND	J1	Z-AA	GND
T2	A00 H	J2	F	A00 H
U1	+3			
U2	INIT H	J1	N	INIT H
V1	EC INC ENB H	J1	J	WC INC ENB H
V2	GND	J1	BB	GND

Table B-1 Signal Cross-Reference DR11-B DR11-W (Cont)

SLOT D

DR11-B			DR11-W	
PIN	**SIGNAL**	**J**	**PIN**	**SIGNAL**
A1	BA INC ENB H	J2	J	BA INC ENB H
A2	+5			
B1	SPARE			
B2	GND	J2	A-S	GND
C1	SPARE			
C2	GND	J2	C-U	GND
D1	GND	J2	E-W	GND
D2	SPARE			
E1	GND	J2	H-Y	GND
E2	FNCT1 H	J2	V	FNCT 1 H
F1	C0 CONTROL H	J2	N	C0 CNTL H
F2	C1 CONTROL H	J2	T	C1 CNTL H
H1	FNCT2 H	J2	R	ALCOFNCT 2 H
H2	SINGLE CYCLE H	J1	K	BURST RQ L
J1	READY H	J1	F	READY H
J2	FNCT3 H	J2	L-K	FNCT 3 H
K1	DAT11 OUT H	J1	LL	DO 11 H
K2	DAT15 OUT H	J1	VV	DO 15 H
L1	DAT09 OUT H	J1	FF	DO 09 H
L2	DAT14 OUT H	J1	TT	DO 14 H
M1	DAT07 OUT H	J1	CC	DO 07 H
M2	DAT13 OUT H	J1	RR	DO 13 H
N1	DAT05 OUT H	J1	HH	DO 05 H
N2	DAT12 OUT H	J1	NN	DO 12 H
P1	DAT03 OUT H	J1	MM	DO 03 H
P2	DAT10 OUT H	J1	JJ	DO 10 H
R1	DAT01 OUT H	J1	SS	DO 01 H
R2	DAT08 OUT H	J1	DD	DO 08 H
S1	DAT00 OUT H	J1	UU	DO 00 H
S2	DAT06 OUT H	J1	EE	DO 06 H
T1	GND	J2	M-Z	GND
T2	DAT04 OUT H	J1	KK	DO 04 H
U1	CYCLE REQUEST B H	J1	Z	CYCLE RQ B H
U2	DAT02 OUT H	J1	PP	DO 02 H
V1	GO H	J2	X	GO H
V2	GND	J2	P-AA-BB	GND

APPENDIX C
DR11-B/DR11-W FUNCTIONALITY COMPARISON

Table C-1 DR11-B/DR11-W Functionality Comparison*

ITEM	FUNCTIONALITY	DR11-B	DR11-W	COMMENTS
1	Packaging	4-slot SU	Standard four layer hex module	
2	No. of chips	User 12 M-series modules	125 ICs	
3	UNIBUS approved DRS/RCV on both UNIBUS and external power.	On UNIBUS interface only. 7400 series TTL logic on user interface.	Yes	
4	After initial power up, an interrupt will occur if IE is set	Yes	No	Since there is no impact on user software, this functionality was eliminated on DR11-W. It has no usefulness on user application.
5	No. of user signal	52	53	The signal does not exist in DR11-B and is added to DR11-W for link mode.
6	Specify cable, its length and termination between user and interface	None specified.	BC06R with 120 ohms and 50 ft max	
7	Capable of overlapping DATO cycles	No	Yes	The DR11-W is designed so that when doing a DATO, it can, in same cycle, receive user data/control of next word while processing current one.
8	Capable of buffering all user signals	No	Yes	All user signals must be asserted through entire cycle in DR11-B. DR11-W stored them at beginning of each cycle.

* This table only shows functions that differ in the two interfaces. For any functions not listed, assume the performance to be the same in both interfaces.

Table C-1 DR11-B/DR11-W Functionality Comparison (Cont)

ITEM	FUNCTIONALITY	DR11-B	DR11-W	COMMENTS
9	No. of resisters required	4	7	IDR, ICR and EIR were added to DR11-W; requires no additional UNIBUS address.
10	Cycle repetition rate between user and interface in DATOs	–	20% faster than DR11-B	This is accomplished by item 7.
11	Interprocessor link	Cannot operate link mode with another DR11-B. The link requires DA11-B which consists of 2 DR11-Bs, 2 cables and 2 M7229 modules.	Can operate link mode with another DR11-W or DRV-11B. The link requires 1 DR11-Ws (or 1 DR11-W and 1 DRV11-B) and 2 cables.	
12	Block and burst transfers in interprocessor link	DA11-B does block transfers only.	Can do both.	DR11-W can do either two-cycle or N-cycle burst in link mode.
13	Method of checking maintenance mode operation	Use diagnostic with test module in SU. This requires FS call.	User diagnostic with logically built-in maintenance mode (no FS call). Use diagnostic with jumper cable on module (FS call required).	The methods used in DR11-W reduce FS calls.
14	No. of user signals untested in maintenance mode	8	None	These eight signals are either tied to gnd, +3 Vdc, or left unconnected.
15	User signals CYCLE RQ A,B	Must be received as a low-to-high going pulse only.	May be received as a low-to-high going pulse or level.	The trailing edge of CYCLE RQ causes DMA transfers in DR11-B.
16	Implementation method of UNIBUS and vector address	Use hard wire jumpers.	Use switches.	
17	Alteration of BR priority level	Rewire SU backplane.	Replace with another plug.	
18	AC Loads	9.1	4.2	
19	Reliability delay line vs RC circuits	Uses RC circuits to generate SSYN MSYN and other critical signals.	Uses delay lines to generate SSYN MSYN and other critical signals.	
20	Release Bus gracefully upon powerfail	If powerfailure occurs in CPU, it does not allow its bus BBSY to be released. The bus is only released by INIT, resulting in unexpected DMA termination.	DR11-W will terminate its DMA transfers and release its Bus BBSY at end of current transfer, if powerfail occurs	

Table C-1 DR11-B/DR11-W Functionality Comparison (Cont)

ITEM	FUNCTIONALITY	DR11-B	DR11-W	COMMENTS
21	Additional functions performed by CSR bits 00, 13, 14 and 15	**BIT 00 GO** 1. Causes a pulse to be sent to user, indicating a new command has been issued. 2. Always read as a 0.	**BIT 00 GO/REG FLAG** 1. In addition to do what DR11-B does, it is used to indicate a register flag. When set, EIR is read, and clears, CSR is read.	
21		**BIT 13 ATTN** 1. Set and cleared by user only. 2. If ATTN is received during a transfer, DMA operation is abruptly terminated and bad data may result. 3. No visual indication displayed, when it is asserted (either by disconnecting user cable from SU or ATTN has been stuck high).	**BIT 13 ATTN** 1. Set and cleared by user. It is also latched so it is processed at appropriate time and is cleared at start of next transfer, or writing a 0 to it. 2. If ATTN is received during a transfer, DMA operation will terminate at end of current transfer; no bad data should result. 3. ATTN, LED, when lit, indicates that this bit is asserted either by disconnect of user cable from module, or by ATTN being stuck high.	
21		**BIT 14 NEX** 1. Set by nonexistent memory, which indicates that DR11-B did not receive a SSYN response 20 μs after asserting MYSN; cleared by writing a 0 to it.	**BIT 14 NEX** 1. Set by nonexistent memory, which indicates that DR11-W did not receive a SSYN response 13 us (UNIBUS) or 38 μs (11/780 or UBA) after asserting MSYN; cleared by writing a 0 to it or at start of next DMA transfers.	
21		**BIT 15 ERROR** 1. Indicates an error eondition; ATTN or NEX. 2. Clear by removing error conditions; ATTN is cleared by user and NEX by writing a 0 to it.	**BIT 15 ERROR** 1. Indicates an error conditon; (ATTN, NEX, MULTICY RQ, ACLO or PAR ERR). 2. Clear by removing error conditons; all errors are cleared by GO at the start of the next DMA transfers. In addition, ATTN and NEX can also be cleared by writing a 0 to bits 13 and 14 respectively.	

Table C-1 DR11-B/DR11-W Functionality Comparison (Cont)

ITEM	FUNCTIONALITY	DR11-B	DR11-W	COMMENTS
22	BR request initiation	Allows an interrupt to occur when IE sets and one of the following conditons is met: 1) NEX or ATTN is generated; 2) IN NPR environment.	Allows an interrupts to occur when IE sets and one of the following conditions is met: 1) NEX, 2) ATTN, 3) MULTICY RQ, 4) ACLO, or 5) PAR ERR is generated in NPR environment.	
23	Reading ODR for last word of a block of transfers	When doing a block of DATO, CPU can examine last word of the block transfers by reading 7724X6. However, CPU may or may not set last word because user data may have already negated.	When doing a block DATO, CPU can examine last word of the block transfers by reading 7724X6. This can only be done by writing a 1 to bit 15 of CSR. The last word has been latched.	The CPU is guaranteed to retrieve last word in DR11-W. If user has not negated its last word, EIR ENB does not have to be set; therefore, there is no impact on user software.
24	Possible bus hang in burst mode	It is possible for DR11-B to hang bus if SINGLE CYCLE signal is held asserted and successive CYCLE RQ has not come.	DR11-W eliminates this possibility by BURST DLT time out. The bus is relinquished unconditionally at end of time out.	
25	Add another CSR register	–	An ERROR and INFORMATION register (EIR) was added.	
26	DMA burst transfers	It is capable of doing N-cycle burst only with no LED indication.	It is capable of doing N-cycle and two-cycle bursts. The N-cycle operation is indicated by a LED.	
27	Violate UNIBUS Spec	When operating burst mode, BUS SACK is negated immediately after BUS BBSY is asserted.	When operating burst mode, BUS SACK is negated during the last cycle of a block of transfers.	Negating BUS SACK at the beginning of a block of transfers does not allow CPU to make a true bus arbitration.

Reader's Comments

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